Recommendation X.22

MULTIPLEX DTE/DCE INTERFACE FOR USER CLASSES 3–6

Geneva, 1980, amended at Melbourne, 1988)

The CCITT,

considering

(a) that Recommendations X.1 and X.2 define the services and facilities to be provided by a public data network;

(b) that Recommendation X.21 defines the interface between a Data Terminal Equipment (DTE) and Data Circuit–terminating Equipment (DCE) for synchronous operation on public data networks;

(c) that it is desirable for characteristics of the interface carrying a multiplexed bit stream between a DTE and a multiplex DCE of a public data network to be standardized;

unanimously declares

that the interface between the DTE and the DCE in a public data network using a multiplexed channel configuration employing synchronous transmission should be as defined in this Recommendation.

1 Scope

1.1 This Recommendation defines the interface between a DTE and a multiplex DCE, operating at 48 000 bit/s and multiplexing a number of Recommendation X.21 subscriber channels employing synchronous transmission.

1.2 The number of Recommendation X.21 subscriber channels is limited by the number of subscriber channels allowed in the network multiplex structure (see § 4).

1.3 The provision of all services supported by Recommendation X.21 is possible.

2 DTE/DCE physical interface elements (see Table 1/X.22)

2.1 *Electrical characteristics*

The electrical characteristics of the interchange circuits at both the DCE side and the DTE side of the interface will comply with Recommendation X.27 with implementation of the cable termination in the load.

2.2 *Mechanical characteristics*

Refer to ISO 4903 (15–pole DTE/DCE interface connector and contact number assignments) for mechanical arrangements.

2.3 *Functional characteristics of the interchange circuits*

Definitions of the interchange circuits G, T, R, C, I, S and F are given in Recommendation X.24 and in § 4 below.

TABLE 1/X.22

Interchange circuit	Name	Direction		Remark
		to DCE	from DCE	
G	Signal ground or common return			see Note
T	Transmit	X		
R	Receive		X	
C	Control	X		
I	Indication		X	
S	Signal element timing		X	
F	Frame start identification		X	

Note – This conductor may be used to reduce environmental signal interference at the interference. In the case of shielded interconnecting cable, the additional connection considerations are part of Recommendation X.24 and ISO 4903.

2.4 *Call control and failure detection procedures*

Call control and *failure detection* procedures shall operate as specified in Recommendation X.21 on each subscriber channel independent of other subscriber channels.

2.4.1 *Quiescent states*

The quiescent states shall be in accordance with Recommendation X.21, § 2.5.

2.4.2 *Failure detection*

See Recommendation X.27, § 9 for association of the receiver circuit failure detection types.

2.4.2.1 *Fault conditions on interchange circuits*

The DTE should interpret a fault condition on circuit R as r = 0 on all channels using failure detection type 2, a fault condition on circuit I as i = OFF on all channels using failure detection type 1, and a fault condition on both circuits R and I as r = 0, i = OFF *(DCE not ready)* on all channels.

Alternatively a fault condition on one of these circuits, R or I, may be interpreted by the DTE as r = 0, i = OFF *(DCE not ready)*, using failure detection type 3.

The DCE will interpret a fault condition on circuit T as t = 0 on all channels using failure detection type 2, a fault condition on circuit C as c = OFF on all channels using failure detection type 1, and a fault condition on both circuits T and C as t = 0, c = OFF on all channels *(DTE uncontrolled not ready)*.

Alternatively, a fault condition on one of these circuits, T or C, may be interpreted by the DCE as t = 0, c = OFF *(DTE uncontrolled not ready)*, using failure detection type 3.

2.4.2.2 *DCE fault condition*

Indication of the DCE failure condition shall be in accordance with Recommendation X.21, § 2.6.2.

A DCE failure condition may effect all subscriber channels at the DTE/DCE interface.

2.4.2.3 *Signal element timing provision*

The provision of signal element timing shall be in accordance with Recommendation X.21, § 2.6.3.

2.4.3 *Elements of the call control phase*

The elements of the call control phase, for each channel, shall be in accordance with Recommendation X.21, § 4 with the exception that byte timing is not used.

2.4.4 *Data transfer phase*

The data transfer phase, for each channel, shall be in accordance with Recommendation X.21, § 5.

2.4.5 *Clearing phase*

The clearing phase, for each channel, shall be in accordance with Recommendation X.21, § 6.

3 Alignment of call control characters and error checking

3.1 *Character alignment*

For the interchange of information between the DTE and the DCE for call control purposes, it is necessary to establish correct alignment of characters. Each sequence of call control characters to and from the DCE shall be preceded by two or more contiguous 1/6 (“SYN”) characters.

3.1.1 Certain Administrations will require the DTE to align call control characters transmitted from the DTE to either SYN characters delivered to the DTE or to the signals on the *frame start identification* interchange circuit (F).

3.1.2 Certain Administrations will permit call control characters to be transmitted from the DTE independently of the SYN characters delivered to the DTE.

3.2 *Error checking*

Odd parity according to Recommendation X.4 applies for the interchange of IA5 characters for call control purposes.

4 Multiplex structure

Depending on the multiplex structure used by the network, the structure of the multiplexed bit stream will be one of two different types.

4.1 *Multiplex structure in networks providing 6 bit–bytes*

The DCE shall deliver to and receive from the DTE a 6–bit byte interleaved multiplexed bit stream containing a number of subscriber channels. The allocation of the subscriber channels should be:

5 channels (phases)	of 9600 bit/s or
10 channels	of 4800 bit/s or
20 channels	of 2400 bit/s or
80 channels	of 600 bit/s or

an appropriate mix of channel data signalling rates having an aggregate bit rate of 48 kbit/s.

The multiplex structure is divided into five phases of 9600 bit/s, where each phase shall be homogeneous with regard to the subscriber data signalling rates.

4.1.1 *Interchange circuits and interface signalling scheme*

The interchange circuits between the DTE and the DCE are shown in Figure 1/X.22 and a timing diagram for the signals is given in Figure 2/X.22.

The signalling over the interchange circuits is as follows.

The transmit (T) and receive (R) circuits will convey in one time slot six consecutive user data bits for one subscriber channel (see Figure 2/X.22).

The control (C) and indication (I) circuits will convey the appropriate signal levels in accordance with Recommendation X.21 for the data channel which in the same time slot have bits conveyed over the respective data circuits.

Change of condition on circuit C shall take place at the OFF to ON transition of circuit S at the beginning of the first bit in the 6–bit byte. The condition on circuit C shall be steady for the whole 6–bit byte.

Change of condition on circuit I will take place at the OFF to ON transition of circuit S at the beginning of the first bit in the 6–bit byte and the condition will be steady for the whole 6–bit byte.

The signal element timing (S) will operate for continuous isochronous transmission at 48 kbit/s.

The *frame start identification* circuit (F) will indicate the frame start with an OFF condition appearing in the last bit of each frame. For networks using Recommendation X.50 division 2 multiplexing, the frame length will be 480 bits. For networks using Recommendation X.50 division 3 multiplexing in which the user rate of 600 bit/s is not included, the frame length will be 120 bits.

4.2 *Multiplex structure in networks providing 8–bit bytes*

The DCE shall deliver to and receive from the DTE an 8–bit byte interleaved multiplexed bit stream containing a number of subscriber channels. The allocation of the subscriber channels should be:

5 channels (phases)	of 9600 bit/s or
10 channels (phases)	of 4800 bit/s or
20 channels (phases)	of 2400 bit/s or
80 channels (phases)	of 600 bit/s or

an appropriate mix of channel data signalling rates having an aggregate bit rate of 48 kbit/s.

The multiplex bit stream is divided into five phases of 9600 bit/s, where each phase shall be homogeneous with regard to the subscriber data signalling rates.

4.2.1 *Interchange circuits and interface signalling scheme*

The interchange circuits between the DTE and DCE are shown in Figure 1/X.22 and a timing diagram for the signals is given in Figure 3/X.22. The signalling over the interchange circuits is as follows.

The transmit (T) and receive (R) circuits will convey in one time slot eight consecutive user data bits for one subscriber channel (see Figure 3/X.22).

The control (C) and indication (I) circuits will convey the appropriate signal levels in accordance with Recommendation X.21 for the data channel which in the same time slot have bits conveyed over the respective data circuits.

Change of condition on circuit C shall take place at the OFF to ON transition of circuit S at the beginning of the first bit in the 8–bit byte. The condition on circuit C shall be steady for the whole 8–bit byte.

Change of condition on circuit I will take place at the OFF to ON transition of circuit S at the beginning of the first bit in the 8–bit byte and the condition will be steady for the whole 8–bit byte.

The signal element timing (S) will operate for continuous isochronous transmission at 48 kbit/s.

The frame start identification circuit (F) will indicate the frame start with an OFF condition appearing in the position of the last bit of each 640–bit frame. As an optional facility each frame start could be followed by a code which will indicate the actual channel allocation. This facility is for further study.

5 Test loops

Establishment of test loops for DTE tests and network maintenance is for further study.

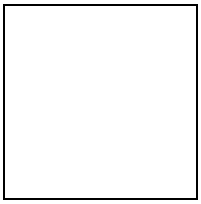

FIGURE 1/X.22 CCITT-38310

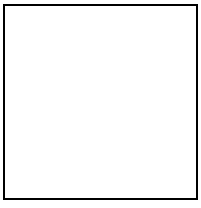

FIGURE 2/X.22 CCITT-38320

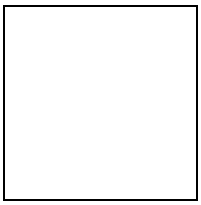

FIGURE 3/X.22 CCITT-38330