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DATA COMMUNICATION OVER THE TELEPHONE NETWORK

A 48/56/64 kbit/s DATA CIRCUIT TERMINATING EQUIPMENT STANDARDIZED FOR USE ON DIGITAL POINT-TO-POINT LEASED CIRCUITS

ITU-T Recommendation V.38

(Previously "CCITT Recommendation")

FOREWORD

The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the International Telecommunication Union. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, established the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

ITU-T Recommendation V.38 was prepared by the ITU-T Study Group XVII (1988-1993) and was approved by the WTSC (Helsinki, March 1-12, 1993).

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NOTES

1 As a consequence of a reform process within the International Telecommunication Union (ITU), the CCITT ceased to exist as of 28 February 1993. In its place, the ITU Telecommunication Standardization Sector (ITU-T) was created as of 1 March 1993. Similarly, in this reform process, the CCIR and the IFRB have been replaced by the Radiocommunication Sector.

In order not to delay publication of this Recommendation, no change has been made in the text to references containing the acronyms "CCITT, CCIR or IFRB" or their associated entities such as Plenary Assembly, Secretariat, etc. Future editions of this Recommendation will contain the proper terminology related to the new ITU structure.

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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A 48/56/64 kbit/s DATA CIRCUIT TERMINATING EQUIPMENT STANDARDIZED FOR USE ON DIGITAL POINT-TO-POINT LEASED CIRCUITS

(Helsinki, 1993)

1 Introduction

This DCE is intended for use on 56-kbit/s and 64-kbit/s digital point-to-point leased circuits other than ISDN. The DCE is specified herein in terms of the DTE-to-DCE interface(s) and features including rate adaptation, end-to-end signalling, testing and multiplexing facilities. The line signal and the signalling rate that is used to connect this type of DCE locally to a 64-kbit/s digital bearer circuit is considered to be a national matter, and is hence not specified herein. The transmission scheme chosen should, however, be capable of providing an octet timing recovery where a rate adaptation as specified in 5 is employed. An octet timing may also become necessary where a rate adaptation of data signalling rates below 48 kbit/s is accomplished (see Appendix III).

The principal characteristics of the DCE are as follows:

a) Duplex mode of operation on digital leased circuits (see Note 1).

b) Gross bit rates of at least 56 kbit/s.

c) Signalling rates up to 56/64 kbit/s.

d) Rate adaptation of 48 kbit/s and 56 kbit/s into 64 kbit/s according to schemes specified in Recommendation V.110.

e) Inclusion of two different types of DTE-DCE functional interfaces.

f) Inclusion of testing facilities.

g) Optional provision of a means to differentiate between user and network data.

h) Optional inclusion of a multiplexer (for further study).

NOTES

1 The implementation of an optional half-duplex mode of operation is for further study.

2 Figure I.1 gives a schematic block diagram of the arrangement of functional blocks (without the multiplexer function) inside the DCE.

3 The term "line signalling rate" as used in the context of this Recommendation refers to the signalling rate at the input of the transmitter of the transmission unit (see Figure I.1).

2 Signalling rates

2.1 Data signalling rates

The recommended data signalling rates (user rates) are synchronous at 48 kbit/s, 56 kbit/s and 64 kbit/s. For certain national applications or upon bilateral agreement between Administrations, also other data signalling rates below 48 kbit/s are applicable (see Appendix III).

2.2 Signalling rates on line

Where the data signalling rate is 48 kbit/s or 56 kbit/s, a rate adaptation to 64 kbit/s as specified in 5 shall be performed at the connection to an international 64 kbit/s bearer circuit. The precise location where this adaptation takes place is a national matter.

NOTE – It should be noted that in some networks the provision of an octet timing may become necessary at the transition from transmission at 56 kbit/s to transmission at 64 kbit/s. Details are outside the scope of this Recommendation, and may be associated with the line signal transmission equipment used. However, a schematic possible scenario is depicted in Figure II.1.

3 Differentiation between user and network data signals

In some cases it may be desirable to provide a means of differentiating between user and network data (e.g. fault detection). The following optional scrambler is provided as a means of accomplishing this differentiation.

NOTE – The potential provision of a scrambler/descrambler inside the transmission unit of the DCE (see Figure I.1) is a national matter, and outside the scope of this Recommendation.

3.1 Scrambler (64 kbit/s only)

Optionally and on bilateral agreement of the Administrations concerned, a self-synchronizing scrambler having the generating polynomial $1 + x^{-18} + x^{-23}$ may be included in the transmitter of the DCE.

The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler data output sequence thus shall be:

$$D_s = D_i \oplus D_s \bullet x^{-18} \oplus D_s \bullet x^{-23}$$

where

D_s is the data sequence at the output of the scrambler;

D_i is the data sequence applied to the scrambler;

D_o is the data sequence at the output of the descrambler (see 3.2);

$\oplus$ denotes modulo 2 addition;

$\bullet$ denotes binary multiplication.

Figure 1 shows a suitable implementation.

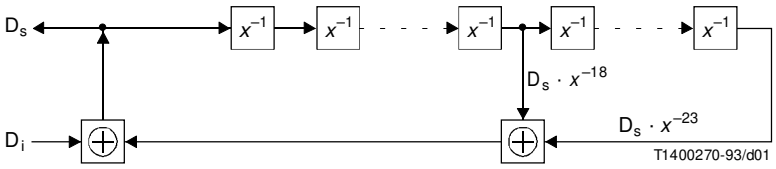


FIGURE 1/V.38

Scrambler

3.2 Descrambler (64 kbit/s only)

Where the optional scrambler specified in 3.1 is provided, also a self synchronizing descrambler having the polynomial $1 + x^{-18} + x^{-23}$ shall be provided in the receiver of the DCE. The message data sequence output by the receiver of the transmission unit (see Figure I.1) shall be effectively multiplied by the generating polynomial $1 + x^{-18} + x^{-23}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by

$$D_o = D_s(1 \oplus x^{-18} \oplus x^{-23})$$

where the notation is defined in 3.1.

Figure 2 shows a suitable implementation.

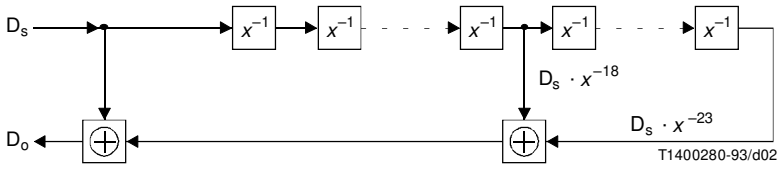


FIGURE 2/V.38

Descrambler

4 Interfaces

One or both types of two functional interfaces shall be provided in the DCE, as specified below. It shall be possible that two DCEs in accordance with this Recommendation can interoperate, where in these DCEs the opposite types of interfaces are employed.

4.1 V.24-type interface

4.1.1 List of interchange circuits

The interchange circuits shall be as in Table 1.

4.1.2 Electrical characteristics

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended as specified below, together with the use of the connector and pin assignment plan specified by ISO 4902 or ISO 2110 AM1.

NOTE – Attention should be drawn to the fact that ISO is in the process of standardizing a shielded connector with smaller physical geometry, that could be used in place of ISO 2110.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

NOTE – In certain instances where V.11 circuits are implemented on both sides of the interface, it may be necessary to add either serial impedance matching resistors or parallel cable terminating resistors as specified in Recommendation V.11 to ensure proper operation of the interchange circuits.

ii) In the case of circuits 105, 106, 107, 108/2 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1 or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies with receivers configured as specified by Recommendation V.10 for category 2.

4.1.3 Operational requirements

The normal operation for this DCE is constant carrier, i.e. the condition of circuit 105 has no influence upon the line signal and upon remote circuit 109. The implementation of an optional half-duplex mode of operation is for further study.

Circuit 106 will follow OFF to ON or ON to OFF transitions on circuit 105 within 0.5 to 3.5 ms (this value is for further study). This time is from the application of an ON or OFF condition on circuit 105.

Optionally, the DCE may provide an end-to-end signalling of local circuit 105 to remote circuit 109. The method used could be as described in Recommendation V.13. Other methods are for further study.

TABLE 1/V.38

V.24-type interface

Interchange circuit		Notes
102	Signal ground or common return	
102a	DTE common return	See Note 1
102b	DCE common return	See Note 1
103	Transmitted data	
104	Received data	
105	Request to send	See Note 2
106	Ready for sending	
107	Data set ready	
108/2	Data terminal ready	See Note 3
109	Data channel received line signal detector	
113	Transmitter signal element timing (DTE source)	See Note 4
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
140	Loopback/Maintenance test	
141	Local loopback	
142	Test indicator	

NOTES

1 Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

2 It shall be possible to apply a permanent ON condition on this circuit inside the DCE.

3 Optional.

4 The use of circuit 113 is for further study, since its application is restricted by the synchronous nature of the network.

Where, depending on the data signalling rate and the line signalling rate a rate adaptation as specified in 5 is employed, both circuits 106 and 109 shall be held in the OFF condition in the event of loss of frame synchronization.

Where the optional scrambler/descrambler function specified in 3 is provided, circuit 109 shall be switched to the OFF condition upon the reception of 256 consecutive bits in the binary ONE condition.

The criteria for the control of circuit 109 depending upon a received line signal or other out of service codes are a national matter, and are outside the scope of this Recommendation.

4.2 X.24-type interface

4.2.1 List of interchange circuits

The interchange circuits for this interface shall be as in Table 2.

TABLE 2/V.38

X.24-type interface

Interchange circuit		Notes
G	Signal ground of common return	See Note 1
G_a	DTE common return	
T	Transmit	
R	Receive	
C	Control	
I	Indication	
S	Signal element timing	See Note 2
X	DTE signal element timing	See Note 3
B	Byte timing	See Notes 4, 5, 6

NOTES

1 This conductor may be used to reduce environmental signal interference at the interface. In the case of shielded interconnecting cable, the additional connection considerations are part of Recommendation X.24 and of ISO 4903.

2 Timing for continuous isochronous data transmission shall be provided.

3 The use and termination of this circuit by the DCE is a national matter, the use being restricted by the synchronous nature of the network.

4 The inclusion of this interchange circuit is optional.

5 It should be noted that this interchange circuit is allocated to the same pole on the connector specified in ISO 4903 as circuit X.

6 The means of providing the byte timing information are a national matter and outside the scope of this Recommendation.

4.2.2 Electrical characteristics

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended as specified below, together with the use of the connector and pin assignment plan specified by ISO 4903.

i) Concerning circuits R, S, T and X, both the generators and the receivers shall be in accordance with Recommendation V.11.

NOTE – In certain instances where V.11 circuits are implemented on both sides of the interface, it may be necessary to add either serial impedance matching resistors or parallel cable terminating resistors as specified in Recommendation V.11 to ensure proper operation of the interchange circuits.

ii) Concerning circuits C and I, generators shall comply with Recommendation V.10 or alternatively V.11. The receivers shall comply with Recommendation V.10, category 1, or Recommendation V.11 without termination.

4.2.3 Operational requirements

No end-to-end signalling of circuit C to remote circuit I is provided with this type of DCE. Instead, local circuit I shall be in the OFF condition when local circuit C is in the OFF condition.

A DCE not ready signal (r = 0, i = OFF) shall be output at the interface:

– in the event of a loss of frame synchronization where, depending on the data signalling rate and the line signalling rate, a rate adaptation as specified in 5 is employed;

– upon the reception of 256 consecutive bits in the binary ONE condition where the optional scrambler/descrambler function specified in 3 is provided.

The DTE should be prepared to receive garbled signals or contiguous binary 1 on circuit R with i = ON, prior to this DCE not ready signal.

The criteria for the control of the interface depending on a received line signal are a national matter, and are outside the scope of this Recommendation.

5 Rate adaptation

The bit rate adaptation for 48 kbit/s shall be as specified in Table 7a/V.110. Octet alignment across the international border is assumed. For national connections, rate adaptation of 48 kbit/s in accordance with Recommendation X.50 *bis* may continue to be used as an alternative.

The rate adaptation of 56 kbit/s shall be as specified in Table 7b/V.110. For national connections, rate adaptation in accordance with Table 7c/V.110 may be used as an alternative.

The precise location where the rate adaptation in accordance with the schemes specified above takes place is a national matter. In some national networks, transmission to the international gateway may be at 56 kbit/s or other line signalling rates or may apply a different adaptation scheme, and rate adaptation in accordance with the schemes specified above, may first be accomplished at the international gateway.

Where the line signalling rate is 56 kbit/s, no adaptation of a data signalling rate of 48 kbit/s is provided.

6 Testing facilities

While it is recognized that the primary means of fault detection/isolation on digital facilities will be accomplished by the network providers through in-service monitoring, the following testing facilities are specified for the case where user initiated fault isolation is desired. The use of the procedure specified in Recommendation V.54 is provided, other methods for providing fault isolation are for further study.

6.1 Test loops

As in Recommendation V.54, the DCEs are referred to hereafter as DCE A and DCE B.

Test loops 2 for the V.24-type interface case, and 2b for the X.24-type interface case, shall be provided. Test loop 3 shall be provided for the V.24-type interface, and one of the test loops 3a or 3b for the X.24-type interface. The precise location of these type-3 loops is beyond the scope of this Recommendation.

The definitions of these test loops are as described in Recommendations V.54 and X.150, respectively. Operation and signalling at the DTE-DCE interfaces of DCE A and DCE B shall be as specified in Recommendations V.54 and X.21, respectively.

6.1.1 Instigation of remote loop 2/2b

The control of loop 2 (loop 2b respectively) shall utilize the preparation and termination phases as specified in Recommendation V.54.

NOTE – Clauses 5, 6 and 7/V.54 describes the automatic control with synchronous DCEs for simple multipoint circuits, point-to-point duplex circuits and tandem circuits. Only the point-to-point duplex circuit case is applicable where in the DCE the X.24-type interface is employed. Application of the two other configurations with the X.24-type interface is for further study.

The instruction of a DCE (DCE A) to instigate a remote loop 2/2b may be manual or automatic. The automatic case shall be upon the recognition of an OFF-to-ON transition on circuit 140 (in the case of the V.24-type interface) or upon the recognition of a Send loop 2 command (state L21, c = OFF, t = 0011) (in the case of the X.24-type interface).

This means, irrespective of the type of interface employed, scrambling of a binary 0 with the polynomial $1 + x^{-4} + x^{-7}$ and transmitting it as though it was introduced to the DCE via circuit 103 or circuit T, respectively.

6.1.2 Instigation of the type-3 loop

The instruction of a DCE to instigate a type-3 loop may be manual or automatic. The automatic case shall be upon the recognition of an OFF-to-ON transition on circuit 141 (in the case of the V.24-type interface) or upon the recognition of a Send loop 3 command (state L31, c = OFF, t = 00001111) (in the case of the X.24-type interface).

6.2 Self tests

The provision of the self-test function specified herein is optional.

The tests described hereafter (in 6.2.1 and 6.2.2) employ an internally generated data pattern that is typically controlled by a switch on the DCE. It shall be possible to perform these tests with or without the DCE being connected to a DTE.

Upon activation of the self-test function, an internally generated data pattern at the selected user signalling rate shall be transmitted as though it was introduced to the DCE via circuit 103 or circuit T, respectively (see Figure I.1). An error detector, capable of identifying errors in the test pattern, shall be connected to the received data path. How the presence of errors is indicated is beyond the scope of this Recommendation.

NOTE – The test pattern has no end-to-end bearing. Its specification is therefore not part of this Recommendation. Examples for test patterns may be alternative binary ONEs and ZEROs (reversals) or the 511-bit test pattern in accordance with Recommendation O.153.

During any self-test mode, interchange circuits 103, 105 and 108/2 (where provided) at the V.24-type interface, and interchange circuits T and C at the X.24-type interface, shall be ignored.

At the V.24-type interface, all generating interchange circuits except 114 (if used), 115 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and shall use its internal clock.

At the X.24-type interface, the DCE shall signal state DCE not ready (r = 0, i = OFF) to the DTE. If circuit X is used, the DCE shall disregard this interchange circuit and shall use its internal clock.

6.2.1 Self test with the type-3 loop

The type-3 loop as defined in Recommendations V.54 and X.150, respectively, shall be activated in the DCE. The self-test function shall be activated, and the DCE operation shall be as described in 6.2.

6.2.2 Self test with remote loop 2/2b

The DCE shall be conditioned to instigate a loop 2/2b at the remote DCE as specified in 6.1.1. The self-test function shall be activated, and the DCE operation shall be as described in 6.2.

7 Multiplexing

A multiplexing option may be included to combine subchannels into a single aggregate bit stream for transmission. The method for the identification of the individual data subchannels is for further study.

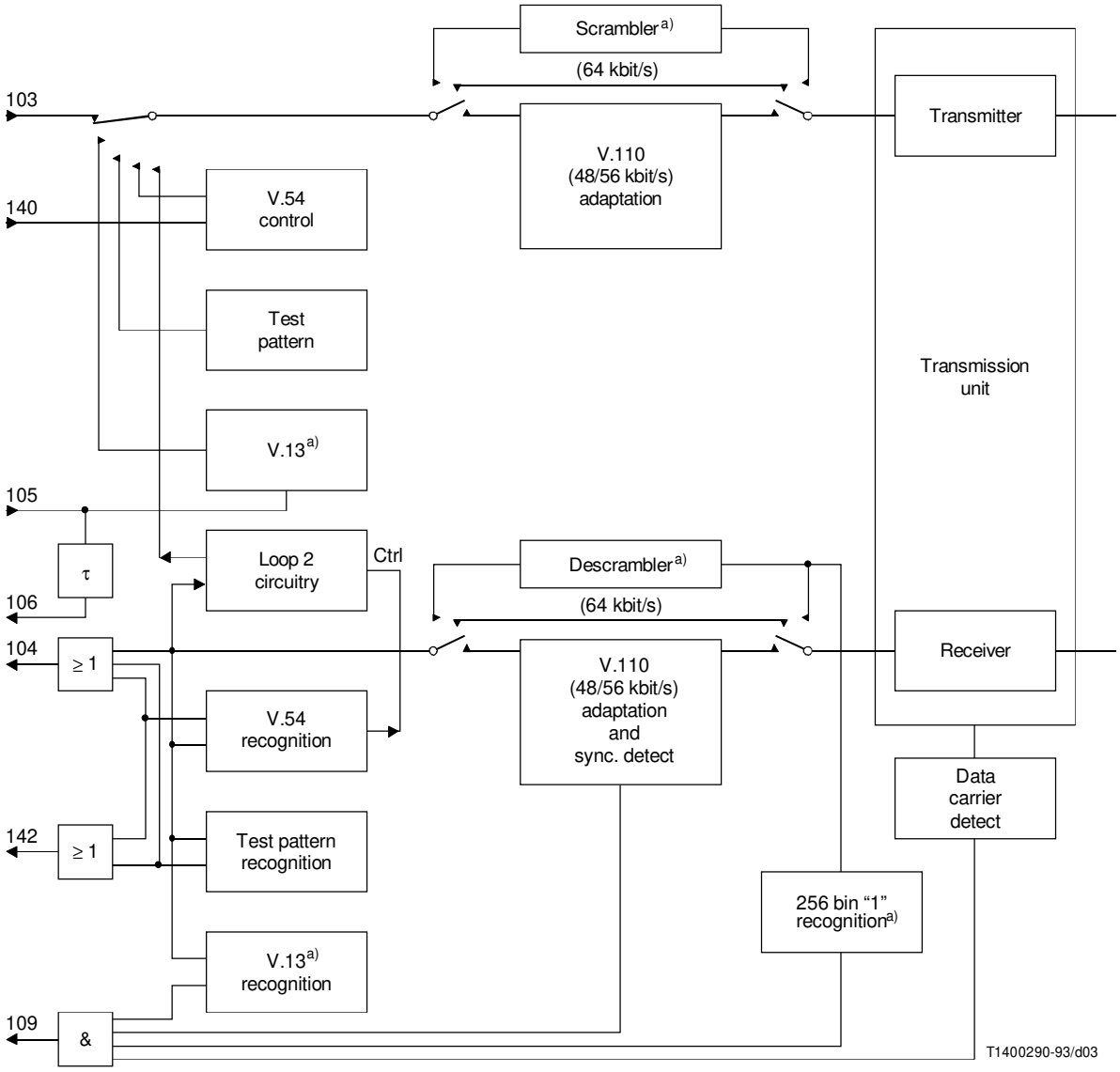
Appendix I

Functional block diagram

(This appendix does not form an integral part of this Recommendation)

Figure I.1 gives an example for a simplified functional block diagram of a DCE in accordance with this Recommendation, that contains all functional blocks specified in the main part of this Recommendation. For this example it was assumed that the DCE would be capable of transmitting at 64 kbit/s and of converting user data rates of 48 kbit/s and 56 kbit/s to this data signalling rate.

The transmission unit contains all functions of a (typically baseband) transmitter and a receiver, which are necessary to interface the DCE to the cable plant of the respective national network. Details are a national matter. For this example it was assumed that the transmission unit is inside the DCE, and interworks with a transmission unit which is installed at the other end of the local loop (see also Appendix II).



a) Optional.

FIGURE I.1/V.38

An example for a simplified functional block diagram

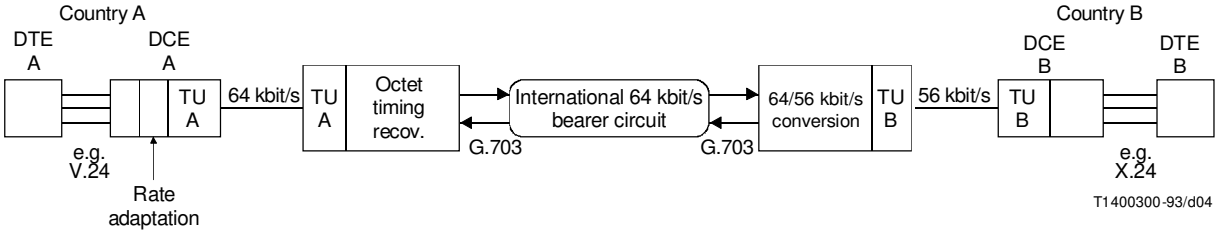
Appendix II

Connection schematic

(This appendix does not form an integral part of this Recommendation)

Figure II.1 provides an example of a 56 kbit/s digital leased circuit between two countries, where 56 kbit/s and 64 kbit/s, respectively, user signalling rates are employed.

DCE B does not conform to this Recommendation.



TU Transmission unit

FIGURE II.1/V.38

Appendix III

Rate adaptation of data signalling rates below 48 kbit/s

(This appendix does not form an integral part of this Recommendation)

The following information is provided as an example where it is intended to utilize the DCE specified in the main part of this Recommendation for user signalling rates below 48 kbit/s (without sub-rate multiplexing). Alternative adaptation schemes may also be used in some countries.

III.1 Data signalling rates

In addition to the data signalling rates specified in the main part of this Recommendation, the following data signalling rates may be provided at the DTE-DCE interface:

- 2400 bit/s;
- 4800 bit/s;
- 9600 bit/s;
- 19 200 bit/s.

III.2 Rate adaptation

The rate adaptation should be accomplished as specified in Recommendation V.110. The following tables shall be applied for the data signalling rates of the incoming signal:

- 2400 bit/s: Table 6c/V.110;
- 4800 bit/s: Table 6e/V.110;
- 9600 bit/s: Table 6e/V.110;
- 19 200 bit/s: Table 6e/V.110.

III.3 Interfaces

III.3.1 Interchange circuits

The V.24/V.28-type interface shall be provided in the DCE. The interchange circuits shall be as in Table 1.

III.3.2 Operational requirements

Optionally, the DCE may provide an end-to-end signalling of local circuit 105 to remote circuit 109. The SB group of S bits as specified in 2.1.2.3/V.110 shall be used to convey the conditions of circuits 105/109.

Optionally, the DCE may provide an end-to-end signalling of local circuit 108/2 to remote circuit 107. The SA group of S bits as specified in 2.1.2.3/V.110 shall be used to convey the condition of circuit 108/2 to circuit 107.

In the event of loss of frame synchronization, both circuits 106 and 109 shall be held in the OFF condition. The requirements specified in 4.1.5/V.110, item e) do not apply.

III.3.3 Testing facilities

Integration of loop 2:

The E4 bit as specified in 2.1.2.3/V.110 shall be used to convey the condition of circuit 140. The remote DCE, upon recognition of status bit E4, will establish loop 2 and turn status E5 bit to the ON condition (binary ZERO) in the transmitted frame. The local DCE, upon recognition of status E5 bit being in the ON condition will switch on a visual indicator.

The control of circuits 107 and 142 shall be as described in Table 2/V.54.