INTERNATIONAL TELECOMMUNICATION UNION

ITU-T V.11

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

(03/93)

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS OPERATING AT DATA SIGNALLING RATES UP TO 10 Mbit/s

ITU-T Recommendation V.11

(Previously "CCITT Recommendation")

FOREWORD

The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the International Telecommunication Union. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, established the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

ITU-T Recommendation V.11 was revised by the ITU-T Study Group XVII (1988-1993) and was approved by the WTSC (Helsinki, March 1-12, 1993).

NOTES

1 As a consequence of a reform process within the International Telecommunication Union (ITU), the CCITT ceased to exist as of 28 February 1993. In its place, the ITU Telecommunication Standardization Sector (ITU-T) was created as of 1 March 1993. Similarly, in this reform process, the CCIR and the IFRB have been replaced by the Radiocommunication Sector.

In order not to delay publication of this Recommendation, no change has been made in the text to references containing the acronyms "CCITT, CCIR or IFRB" or their associated entities such as Plenary Assembly, Secretariat, etc. Future editions of this Recommendation will contain the proper terminology related to the new ITU structure.

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS OPERATING AT DATA SIGNALLING RATES UP TO 10 Mbit/s[1)]

(Geneva, 1976; amended Geneva, 1980, at Melbourne, 1988 and Helsinki, 1993)

1 Introduction

This Recommendation deals with the electrical characteristics of the generator, receiver and interconnecting leads of a differential signalling (balanced) interchange circuit with an optional d.c. offset voltage.

The balanced generator and load components are designed to cause minimum mutual interference with adjacent balanced or unbalanced interchange circuits (see Recommendation V.10) provided that waveshaping is employed on the unbalanced circuits.

In the context of this Recommendation, a balanced interchange circuit is defined as consisting of a balanced generator connected by a balanced interconnecting pair to a balanced receiver. For a balanced generator the algebraic sum of both the outlet potentials, with respect to earth, shall be constant for all signals transmitted; the impedances of the outlets with respect to earth shall be equal. The degree of balance and other essential parameters of the interconnecting pair is a matter for further study.

An annex and two appendices are provided to give guidance on a number of application aspects as follows:

Annex A Compatibility with other interfaces.

Appendix I Cable and termination.

Appendix II Multipoint operation.

NOTE – Generator and load devices meeting the electrical characteristics of this Recommendation need not operate over the entire data signalling rate range specified. They may be designed to operate over narrower ranges to satisfy requirements more economically, particularly at lower data signalling rates.

Reference measurements are described which may be used to verify certain of the recommended parameters but it is a matter for individual manufacturers to decide what tests are necessary to ensure compliance with the Recommendation.

2 Field of application

The electrical characteristics specified in this Recommendation apply to interchange circuits operating with data signalling rates up to 10 Mbit/s.

Typical points of application are illustrated in Figure 1.

Whilst the balanced interchange circuit is primarily intended for use at the higher data signalling rates, its use at the lower rates may be necessary in the following cases:

1) where the interconnecting cable is too long for proper unbalanced circuit operation;
2) where extraneous noise sources make unbalanced circuit operation impossible;
3) where it is necessary to minimize interference with other signals.

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1) This Recommendation is also designated as X.27 in the X Series Recommendations.

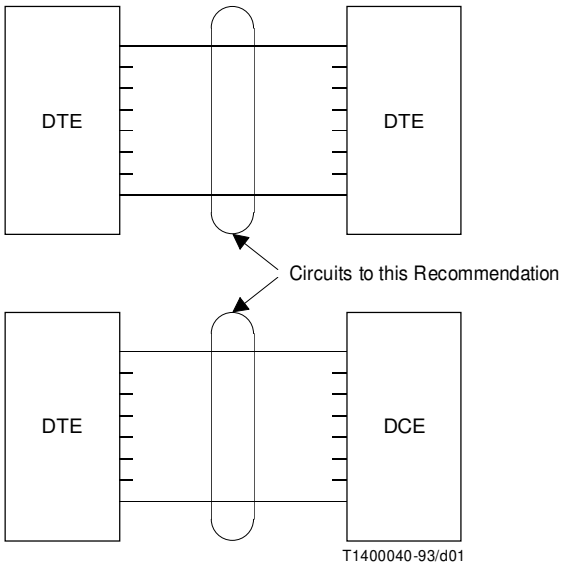


FIGURE 1/V.11

Typical applications of balanced interchange circuits

3 Symbolic representation of interchange circuit

See Figure 2.

The equipment at both sides of the interface may implement generators as well as receivers in any combination. Consequently, the symbolic representation of the interchange circuit, Figure 2 above, defines a generator interchange point as well as a load interchange point.

For data transmission applications, it is commonly accepted that the interface cabling will be provided by the DTE. This introduces the line of demarcation between the DTE plus cable and the DCE. This line is also called the interchange point and physically implemented in the form of a connector. The applications also require interchange circuits in both directions. This leads to an illustration as shown in Figure 3.

4 Generator polarities and receiver significant levels

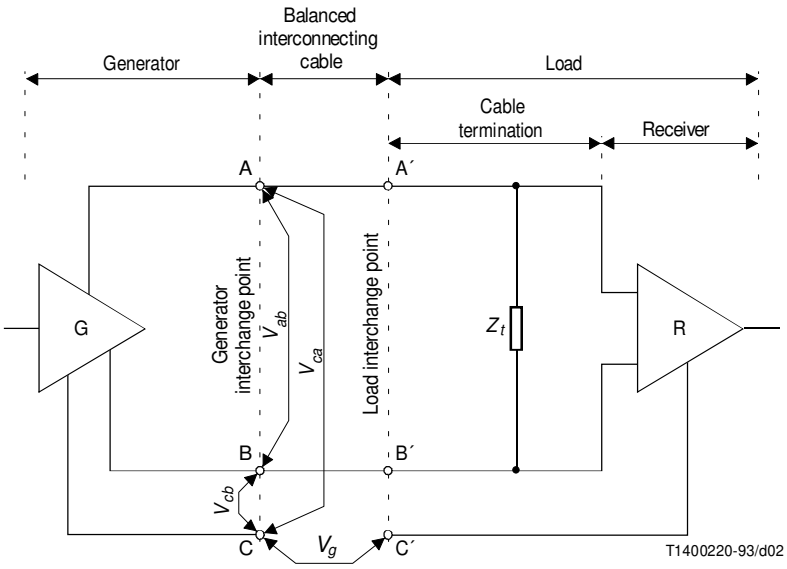
4.1 Generator

The signal conditions for the generator are specified in terms of the voltage between output points A and B shown in Figure 2.

When the signal condition 0 (space) for data circuits or ON for control and timing circuits is transmitted, the output point A is positive with respect to point B. When the signal condition 1 (mark) for data circuits or OFF for control and timing circuits is transmitted, the output point A is negative with respect to point B.

4.2 Receiver

The receiver differential significant levels are shown in Table 1, where $V_{A'}$ and $V_{B'}$ are respectively the voltages at points A′ and B′ relative to point C′.



V_{ab}	Generator output voltage between points A and B
V_{ca}	Generator voltage between points C and A
V_{cb}	Generator voltage between points C and B
Z_t	Cable termination impedance
V_g	Ground potential difference
A, B and A´, B´	Interchange points
C, C´	Zero volt reference interchange points

NOTES

1 Two interchange points are shown. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The electrical characteristics to which the receiver must respond are defined at the "load interchange point".

2 Points C and C´ may be interconnected and further connected to protective ground if required by national regulations.

FIGURE 2/V.11

Symbolic representation of a balanced interchange circuit

5 Generator[2)]

5.1 Resistance and d.c. offset voltage

5.1.1 The total generator resistance between points A and B shall be less than or equal to 100 ohms and be adequately balanced with respect to point C. The degree of balance required, both static and dynamic, is left for further study)

NOTES

1 It is assumed that the value of the dynamic source impedance is in the same range.

2 In the event that reflections are experienced on V.11 circuits, either the use of a terminating network at the receiver (in the range of 120 to 126 ohms) or the use of series resistors (approximately 33 ohms) added to the generator output leads, should alleviate this problem. This latter solution has the addtional benefit of providing protection from over-voltages but creates a problem with meeting the Test-termination measurement specified in 5.2.2.

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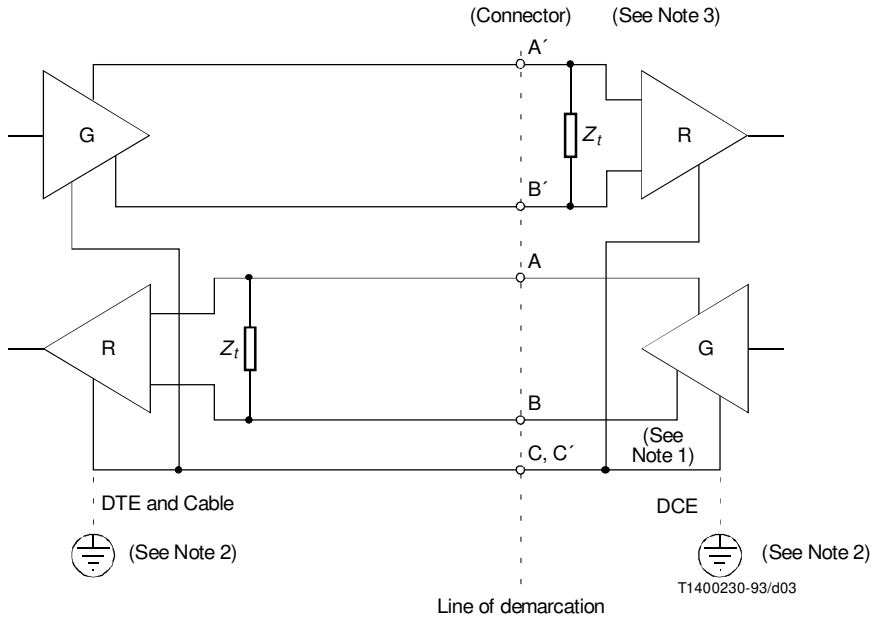
2) For test purposes other than specified in this Recommendation (e.g. signal quality measurement), a transmitter test load of 100 ohms may be used.



NOTES

1 The zero volt reference interchange point C, C´ may be interconnected via the signal ground conductor.

2 Signal ground may be further connected to external protective ground if national regulations require.

3 The type of connector with this electrical characteristic specification depends on the application. ISO specifies, for data transmission over telephone type facilities, a 37-pin connector in ISO 4902 and, for data transmission over data network facilities, a 15-pin connector in ISO 4903.

FIGURE 3/V.11

Practical representation of the interface

TABLE 1/V.11

Receiver differential significant levels

	$V_{A'} - V_{B'} \leq -0.3$ V	$V_{A'} - V_{B'} \geq +0.3$ V
Data circuits	1	0
Control and timing circuits	OFF	ON

5.1.2 The magnitude of the generator d.c. offset voltage (see 5.2.2) shall not exceed 3 V under all operating conditions.

5.2 Static reference measurements

The generator characteristics are specified in accordance with measurements illustrated in Figure 4 and described in 5.2.1 to 5.2.4.

5.2.1 Open-circuit measurement

See Figure 4a).

The open-circuit voltage measurement is made with a 3900-ohm resistor connected between points A and B. In both binary states, the magnitude of the differential voltage (V_0) shall not be more than 6.0 volts, nor shall the magnitude of V_{0a} and V_{0b} be more than 6.0 volts.

5.2.2 Test-termination measurement

See Figure 4b).

With a test load of two resistors, each 50 ohms, connected in series between the output points A and B, the differential voltage (V_t) shall not be less than 2.0 volts or 50% of the magnitude of V_0, whichever is greater. For the opposite binary state the polarity of V_t shall be reversed ($-V_t$) The difference in the magnitudes of V_t and $-V_t$ shall be less than 0.4 volt. The magnitude of the generator offset voltage V_{0s} measured between the centre of the test load and point C shall not be greater than 3.0 volts. The magnitude of the difference in the values of V_{0s} for one binary state and the opposite binary state shall be less than 0.4 volt.

NOTE – Under some conditions this measurement does not determine the degree of balance of the internal generator impedances to point C. It is left for further study whether additional measurements are necessary to ensure adequate balance in generator output impedances.

5.2.3 Short-circuit measurement

See Figure 4c).

With the output points A and B short-circuited to point C, the current flowing through each of the output points A or B in both binary states shall not exceed 150 milliamperes.

5.2.4 Power-off measurements

See Figure 4d).

Under power-off condition with voltages ranging between +0.25 volt and –0.25 volt applied between each output point and point C, as indicated in Figure 4d), the magnitude of the output leakage currents (I_{xa} and I_{xb}) shall not exceed 100 microamperes.

5.3 Dynamic voltage balance and rise time measurements

See Figure 5.

With the measurement configuration shown in Figure 5, a test signal with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 V_{ss} within 0.1 of t_b or 20 nanoseconds, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{ss} from the steady state value.

The resultant voltage due to imbalance (V_E) shall not exceed 0.4 V peak-to-peak.

6 Load

6.1 Characteristics

The load consists of a receiver (R) and an optional cable termination resistance (Z_t) as shown in Figure 2. The electrical characteristics of the receiver are specified in terms of the measurements illustrated in Figures 6, 7 and 8 and described in 6.2, 6.3 and 6.4. A circuit meeting these requirements results in a differential receiver having a high input impedance, a small input threshold transition region between –0.3 and +0.3 volts differential, and allowance for an internal bias voltage not to exceed 3 volts in magnitude.

The receiver is electrically identical to that specified for the unbalanced receiver in Recommendation V.10.

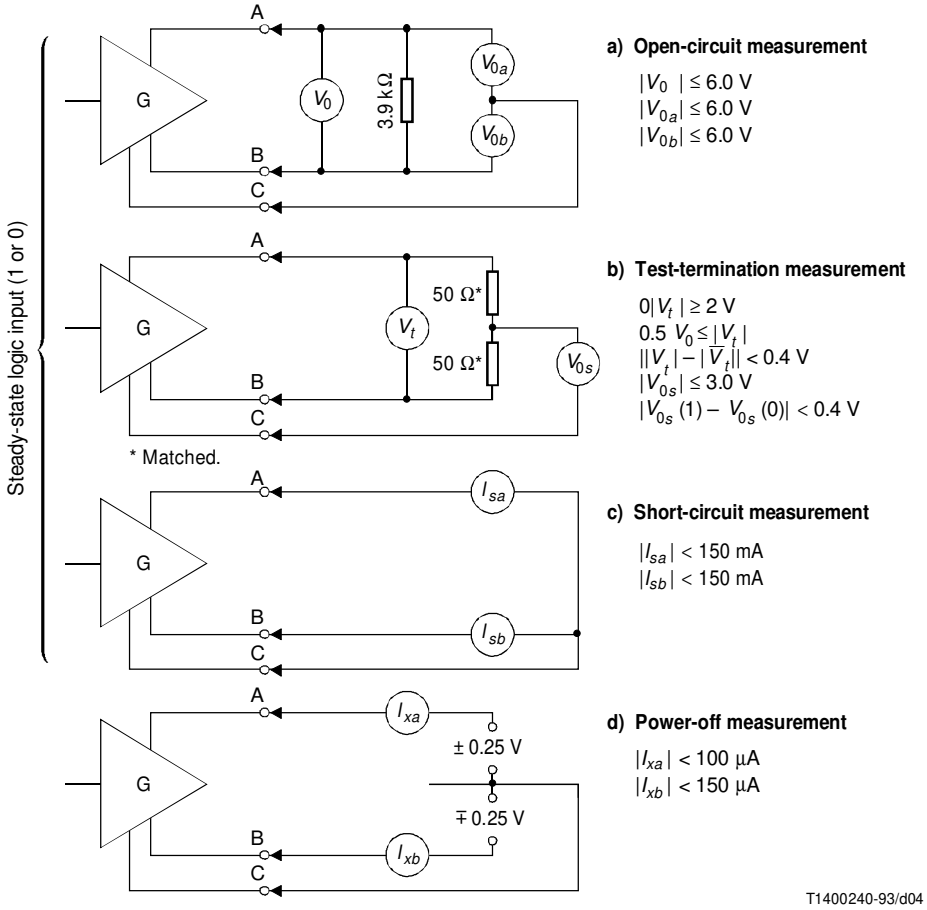


FIGURE 4/V.11

Generator-parameter reference measurements

6.2 Receiver input voltage – Current measurements

See Figure 6.

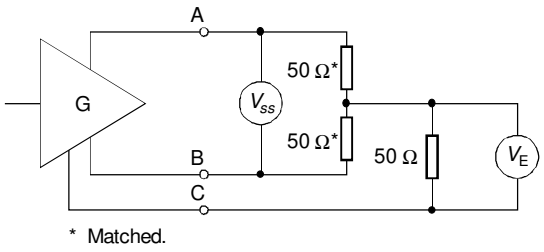
With the voltage V_{ia} (or V_{ib}) ranging between –10 volts and +10 volts, while V_{ib} (or V_{ia}) is held at 0 volt, the resultant input current I_{ia} (or I_{ib}) shall remain within the shaded range shown in Figure 6. These measurements apply with the power supply of the receiver in both the power-on and power-off conditions.

6.3 D.c. input sensitivity measurements

See Figure 7.

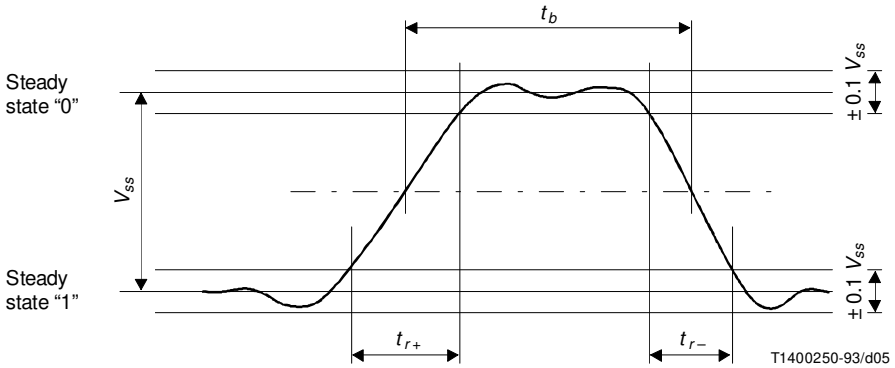
Over the entire common mode voltage (V_{cm}) range of +7 volts to –7 volts, the receiver shall not require a differential input voltage (V_i) of more than 300 millivolts to assume correctly the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state.

The maximum voltage (signal plus common mode) present between either receiver input and receiver ground shall not exceed 10 volts nor cause the receiver to malfunction. The receiver shall tolerate a maximum differential voltage of 12 volts applied across its input terminals without being damaged.



V_E < 0.4 V peak-to-peak (provisional)

V_{ss} Voltage difference between steady-state signal conditions



t_b Nominal duration of the test signal element

for $t_b \geq 200$ ns, $t_r \leq 0.1\ t_b$

for $t_b < 200$ ns, $t_r \leq 20$ ns

FIGURE 5/V.11

Generator dynamic balance and rise-time measurements

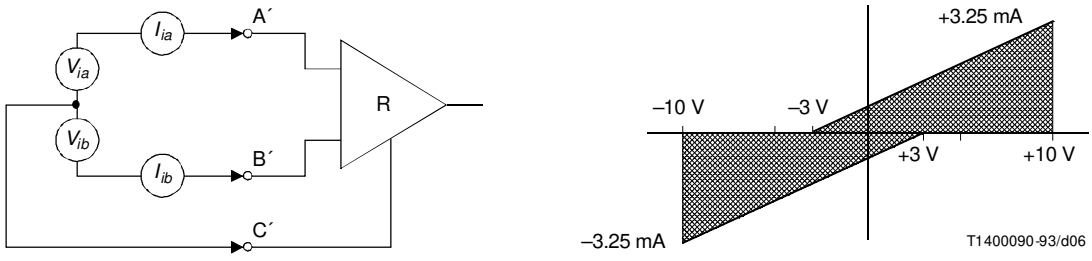
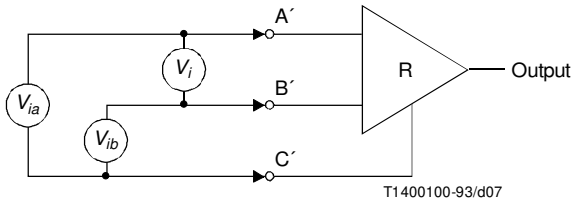


FIGURE 6/V.11

Receiver input voltage-current measurements

In the presence of the combination of input voltages V_{ia} and V_{ib} specified in Figure 7, the receiver shall maintain the specified output binary state and shall not be damaged.

NOTE – Designers of equipment should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving equipment; therefore, appropriate techniques should be implemented to prevent such behaviour. For example, adequate hysteresis may be incorporated in the receiver to prevent such conditions.



Applied voltages		Resulting input voltage V_i	Output binary state	Purpose of measurement
V_{ia}	V_{ib}			
–12 V 0 V +12 V 0 V	0 V –12 V 0 V +12 V	–12 V +12 V +12 V –12 V	(Not specified)	To ensure no damage to receiver inputs
+10 V +4 V –10 V –4 V	+4 V +10 V –4 V –10 V	+6 V –6 V –6 V +6 V	0 1 1 0	To guarantee correct operation at V_i = 6 V (maintain correct logic state)
				300 mV threshold measurement
+0,30 V 0 V	0 V +0,30 V	+0,3 V –0,3 V	0 1	} V_{cm} = 0 V
+7,15 V +6,85 V	+6,85 V +7,15 V	+0,3 V –0,3 V	0 1	} V_{cm} = +7 V
–7,15 V –6,85 V	–6,85 V –7,15 V	–0,3 V +0,3 V	1 0	} V_{cm} = –7 V

FIGURE 7/V.11

Receiver input sensitivity measurement

6.4 Input balance test

See Figure 8.

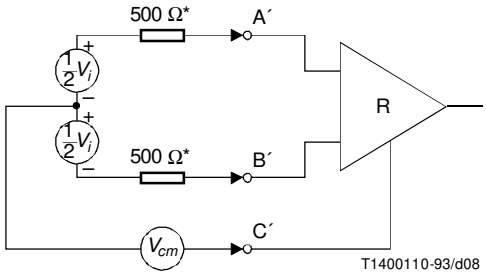
The balance of the receiver input resistance and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the conditions shown in Figure 8 and described as follows:

a) with V_i = +720 millivolts and V_{cm} varied between –7 and +7 volts;

b) with V_i = –720 millivolts and V_{cm} varied between –7 and +7 volts;

c) with V_i = +300 millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study);

d) with V_i = –300 millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable data signalling rate (this condition is provisional and subject to further study).



* Matched.

FIGURE 8/V.11

Receiver input balance test

6.5 Terminator

The use of a cable terminating impedance (Z_t) is optional depending upon the specific environment in which the interchange circuit is employed (see Appendix I). In no case shall the total load resistance be less than 100 ohms.

7 Environmental constraints

In order to operate a balanced interchange circuit at data signalling rates ranging between 0 and 10 Mbit/s, the following conditions apply:

1) For each interchange circuit a balanced interconnecting pair is required.

2) Each interchange circuit must be appropriately terminated (see Appendix I).

3) The total common-mode voltage at the receiver must be less than 7 volts peak.

The common mode voltage at the receiver is the worst case combination of:

a) generator-receiver ground-potential difference (V_g, Figure 2);

b) longitudinally induced random noise voltage measured between the receiver points A′ or B′ and C′ with the generator ends of the cable A, B and C joined together; and

c) generator d.c. offset voltage, if any.

Unless the generator is of a type which generates no d.c. offset voltage, the sum of a) and b) above, which is the element of the common mode voltage due to the environment of the interchange circuit, must be less than 4 volts peak.

8 Circuit protection

Balanced generator and load devices complying with this Recommendation shall not be damaged under the following conditions:

1) generator open circuit;

2) short-circuit between the conductors of the interconnecting cable;

3) short-circuit between either or both conductors and point C or C′.

The above faults 2) and 3) might cause power dissipation in the interchange circuit devices to approach the maximum power dissipation that may be tolerable by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators and receivers are implemented in a single IC package, only one such fault per package might be tolerable at any one time without damage occurring.

The user is also cautioned that the generator and receiver devices complying with this Recommendation might be damaged by spurious voltages applied between their input or output points and points C or C′ (Figure 2). In those applications where the interconnecting cable may be inadvertently connected to other circuits, or where it may be exposed to a severe electromagnetic environment, protection should be employed.

9 Detection of generator power-off or circuit failure

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator power-off condition;

2) receiver not interconnected with a generator;

3) open-circuited interconnecting cable;

4) short-circuited interconnecting cable;

5) input signal to the load remaining within the transition region (± 300 millivolts) for an abnormal period of time.

When detection of one or more fault conditions is required by specific applications, additional provisions are required in the load and the following items must be determined:

a) which interchange circuits require fault detection;

b) what faults must be detected;

c) what action must be taken when a fault is detected, e.g. which binary state must the receiver assume?

The interpretation of a fault condition by a receiver (or load) is application dependent. Each application may use a combination of the following classification:

Type 0 – No interpretation. A receiver or load does not have fault detection capability.

Type 1 – Data circuits assume a binary 1 state. Control and timing circuits assume an OFF condition.

Type 2 – Data circuits assume binary 0 state. Control and timing circuits assume an ON condition.

Type 3 – Special interpretation. The receiver or load provides a special indication for interpreting a fault condition. This special indication requires further study.

The association of the circuit failure detection to particular interchange circuits in accordance with the above types is a matter of the functional and procedural characteristics specification of the interface.

The interchange circuits monitoring circuit fault conditions in the general telephone network interfaces are indicated in Recommendation V.24.

The interchange circuits monitoring circuit fault conditions in public data network interfaces are indicated in Recommendation X.24 [1].

The receiver fault detection type required is specified in the relevant DCE Recommendations.

10 Measurements at the physical interchange point

The following information provides guidance for measurements when maintenance persons examine the interface for proper operation at the interchange point.

10.1 Listing of essential measurements

- the magnitude of the generator d.c. offset voltage under all operating conditions;
- open-circuit measurements;
- test-termination measurement;
- short-circuit measurement;
- dynamic voltage balance and rise time;
- d.c. input sensitivity measurements.

10.2 Listing of optional measurements

- The total generator resistance between points A and B shall be equal to or less than 100 ohms and adequately balanced with respect to point C. (It is left for further study as to the degree of balance required both statically and dynamically);
- power-off measurements;
- receiver input voltage-current measurements;
- input balance test;
- check of the required circuit fault detection (see 9).

The parameters defined in this Recommendation are not necessarily measurable at the physical interchange point. This is for further study.

Annex A

Compatibility with other interfaces

(This annex forms an integral part of this Recommendation)

A.1 Compatibility of Recommendation V.10 and Recommendation V.11 interchange circuits in the same interface

The electrical characteristics of this Recommendation are designed to allow the use of unbalanced (see Recommendation V.10) and balanced circuits within the same interface. For example, the balanced circuits may be used for data and timing whilst the unbalanced circuits may be used for associated control circuit functions.

A.2 Recommendation V.11 interworking with Recommendation V.10

The differential receiver specifications of Recommendation V.10 and this Recommendation are electrically identical. It is therefore possible to interconnect an equipment using Recommendation V.10 receivers and generators on one side of the interface with an equipment using Recommendation V.11 generators and receivers on the other side of the interface. Such interconnection would result in the interchange circuits according to this Recommendation in one direction and interchange circuits according to Recommendation V.10 in the other direction. Where such interworking is contemplated, the following technical considerations must be taken into account.

A.2.1 Interconnecting cable lengths are limited by performance of the circuits working to the Recommendation V.10 side of the interface.

A.2.2 The optional cable termination resistance (Z_t), if implemented, in the equipment using this Recommendation must be removed.

A.2.3 V.10-type receivers shall be of category 1.

A.3 Recommendation V.11 interworking with Recommendation V.35

Equipment having interchange circuits according to this Recommendation is expected to interoperate with practical implementations of the electrical characteristics defined in Appendix II/V.35. Interoperation between a V.35 transmitter and a V.11 receiver will result in shorter cable length than those indicated in Figure I.1. This is due to the fact that the output voltage from the V.35 transmitter loaded by a 100 ohms resistor has a minimum value of 0.44 volts peak/peak, which represents about 1/5 of the voltage of the V.11 transmitter (2 volts), as per Figure 7.

Appendix I

Cable and termination

(This appendix does not form an integral part of this Recommendation)

No electrical characteristics of the interconnecting cable are specified in this Recommendation. Guidance is given herein concerning operational constraints imposed by the length, balance and terminating resistance of the cable.

I.1 Cable

Over the length of the cable, the two conductors should have essentially the same values of:

1) capacitance to ground;

2) longitudinal resistance and inductance;

3) coupling to adjacent cables and circuits.

I.2 Cable length

The maximum permissible length of cable separating the generator and the load in a point-to-point application is a function of the data signalling rate. It is further influenced by the tolerable signal distortion and the environmental constraints such as ground potential difference and longitudinal noise. Increasing the distance between generator and load might increase the exposure to ground potential difference.

As an illustration of the above conditions, the curves of cable length versus data signalling rate in Figure I.1 may be used for guidance.

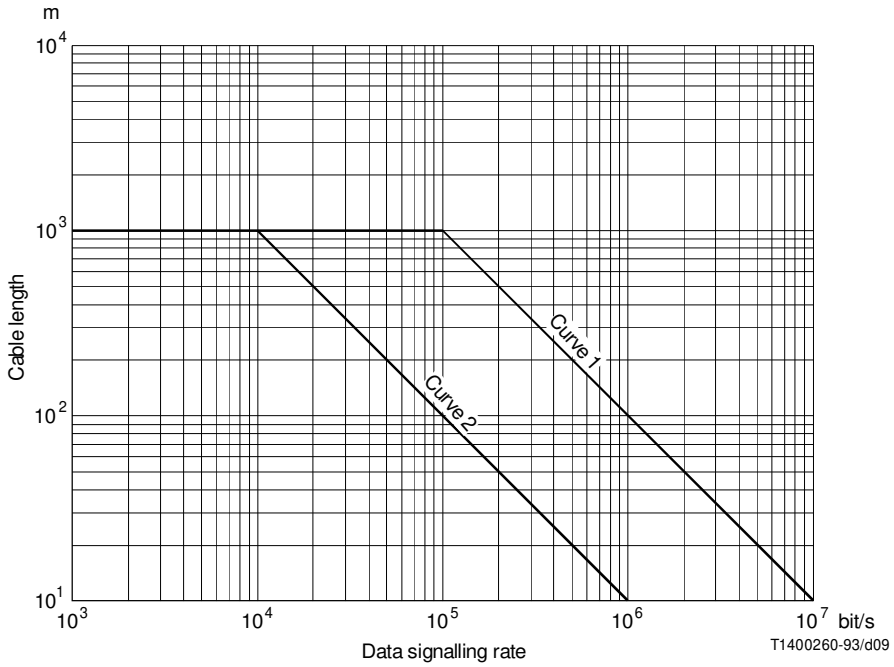
These curves are based upon empirical data using twisted pair telephone cable (0.51-mm wire diameter) both unterminated and terminated in a 100-ohm resistive load. The cable length restrictions shown by the curves are based upon the following assumed signal quality requirements at the load:

1) signal rise and fall time equal to, or less than, one-half the duration of the signal element;

2) a maximum voltage loss between generator and load of 6 dB.

At the higher data signalling rates (see Figure I.1) the sloping portion of the curves shows the cable length limitation established by the assumed signal rise and fall time requirements. The cable length has been arbitrarily limited to 1000 metres by the assumed maximum allowable loss of 6 dB.

These curves assume that the environmental limits specified in this Recommendation have been achieved. At the higher data signalling rates these conditions are more difficult to attain due to cable imperfections and common-mode noise. Operation within the data signalling rate and distance bounds of Figure I.1 will usually ensure that distortion of the signal appearing at the receiver input will be acceptable. Many applications, however, can tolerate much greater levels of signal distortion and in these cases correspondingly greater cable lengths may be employed.



Curve 1 Terminated interchange circuit
Curve 2 Unterminated interchange circuit

FIGURE I.1/V.11

Data signalling rate vs cable length for balanced interchange circuit

Experience has shown that in many practical cases the operating distance at lower signalling rates may extend to several kilometres.

For synchronous transmission where the data and signal element timing are transmitted in opposite directions, the phase relationship between the two may need to be adjusted to ensure conformity with the relevant requirements of signal quality at the interchange point.

I.3 Cable termination

The use of a cable termination resistance (Z_t) is optional and dependent on the specific application. At the higher data signalling rates (above 200 kbit/s) or at any data signalling rate where the cable propagation delay is of the order of half the signal element duration a termination should be used to preserve the signal rise time and minimize reflections. The terminating impedance should match as closely as possible the cable characteristic impedance in the signal spectrum.

Generally, a resistance in the range of 100 to 150 ohms will be satisfactory, the higher values leading to lower power dissipation.

At the lower data signalling rates, where distortion and rise-time are not critical, it may be desirable to omit the termination in order to minimize power dissipation in the generator.

Appendix II

Multipoint operation

(This appendix does not form an integral part of this Recommendation)

For further study. A specification for multipoint operation including the version ISO 8482 is under study.

Reference

[1] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks*, Vol. VIII, Rec. X.24.