INTERNATIONAL TELECOMMUNICATION UNION

CCITT

O.171

THE INTERNATIONAL
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CONSULTATIVE COMMITTEE

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SPECIFICATIONS OF MEASURING EQUIPMENT

TIMING JITTER MEASURING EQUIPMENT FOR DIGITAL SYSTEMS

Recommendation O.171

FOREWORD

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Recommendation O.171 was revised by Study Group IV and was approved under the Resolution No. 2 procedure on the 5th of October 1992.

CCITT NOTE

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Recommendation O.171

TIMING JITTER MEASURING EQUIPMENT FOR DIGITAL SYSTEMS[1)]

(Published 1980; revised 1984, 1988 and 1992)

Abstract

Defines the requirements for an equipment to measure timing jitter on digital equipments operating at hierarchical bit rates between 64 kbit/s and 140 Mbit/s.

Keywords

– jitter measurement;

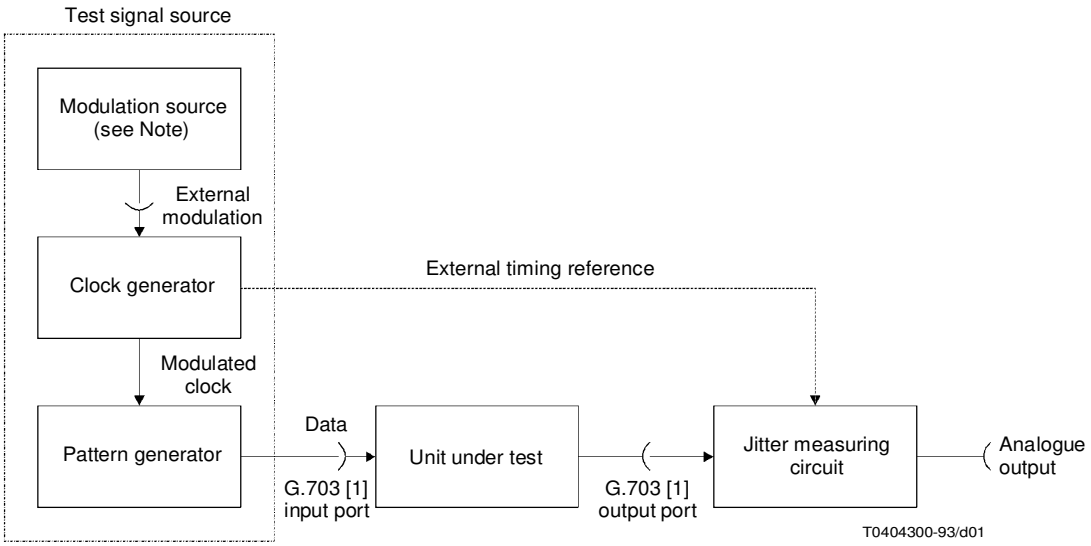
– measurement;

– tester.

1 Introduction

1.1 *General*

1.1.1 The instrumentation specified below will be used to measure timing jitter on digital equipment. This instrumentation, which consists of a jitter measuring circuit and a test signal source, is shown in a general form in Figure 1/O.171. While essential requirements are given for the instrumentation, the realization of the equipment configuration is not covered and should be given careful consideration by the designer and user. An error-ratio meter may also be required for certain types of measurements.



Note – The modulation source, to test to the G.700-series Recommendations, may be provided within the clock generator and/or the pattern generator, or it may be provided separately.

FIGURE 1/O.171

Simplified block diagram for measuring timing jitter

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1) See the Supplement No. 3.8 in the *Blue Book*, Fascicle IV.1.

1.1.2 Certain requirements in this specification are provisional and are still under study. These are individually indicated.

1.1.3 It is recommended that Recommendation G.823 [2] be read in conjunction with this Recommendation.

1.2 *Interfaces*

1.2.1 The instrumentation shall be capable of operating at one or more of the following bit rates and corresponding interface characteristics as described in the appropriate sections of Recommendation G.703 [1]. However, for all bit rates the signal applied to the input of the jitter measuring circuit should be a nominal rectangular pulse. Other signal shapes may produce intersymbol interference thus affecting measurement accuracy.

a) 64 kbits[2)];

b) 1544 kbit/s;

c) 6312 kbit/s;

d) 2048 kbit/s;

e) 8448 kbit/s;

f) 32 064 kbit/s;

g) 44 736 kbit/s;

h) 34 368 kbit/s;

i) 139 264 kbit/s.

1.2.2 As an option, the jitter measuring circuit shall be capable of measuring jitter at a clock output port when such an access is provided on digital equipment.

1.3 *Interface impedances*

1.3.1 The jitter measuring circuit and signal source shall have a return loss better than 20 dB[3)] under the conditions listed in Table 1/O.171.

TABLE 1/O.171

Return loss test conditions

Bit rate (kbit/s)	Test conditions	
64	120 ohms, nonreactive	3 kHz to 300 kHz
1 544	100 ohms, nonreactive	20 kHz to 1.6 MHz
2 048	75/120/130 ohms, nonreactive	40 kHz to 2.5 MHz
6 312	75/110 ohms, nonreactive	100 kHz to 6.5 MHz
8 448	75 ohms, nonreactive	100 kHz to 10 MHz
32 064	75 ohms, nonreactive	500 kHz to 40 MHz
34 368	75 ohms, nonreactive	500 kHz to 40 MHz
44 736	75 ohms, nonreactive	500 kHz to 50 MHz
139 264	75 ohms, nonreactive	7 kHz to 210 MHz

2) References to 64 kbit/s relate to the codirectional interface. Limits for other 64 kbit/s interfaces are under study.

3) In the case of 1544 kbit/s, the signal source shall have the following return loss: 20 kHz to 500 kHz ≥ 14 dB and 500 kHz to 1.6 MHz ≥ 16 dB.

2 Test signal source

Tests of digital equipment may be made with either a jittered or a non-jittered digital signal. This will require the pattern generator, clock generator and modulation source shown in Figure 1/O.171.

2.1 *Modulation source*

The modulation source, testing in conformance with the Series G.700 Recommendations, may be provided within the clock generator and/or pattern generator or it may be provided separately. In this Recommendation it is assumed that the modulation source is sinusoidal.

2.2 *Clock generator*

2.2.1 It shall be possible to phase modulate the clock generator from the modulation source and to indicate the peak-to-peak phase deviation of the modulated signal.

The generated peak-to-peak jitter and the modulating frequencies shall meet the requirements of Figure 2/O.171 and Table 2/O.171.

2.2.2 The modulating input sensitivity of the clock generator shall be at least:

a) 2 volts peak-to-peak into 600 ohms for bit rates up to and including 8448 kbit/s;

b) 1 volt peak-to-peak into 75 ohms for bit rates up to and including 139 264 kbit/s.

2.2.3 The minimum output of the modulated clock signal and the external timing reference signal shall be 1 volt peak-to-peak into 75 ohms.

2.2.4 *Accuracy of the clock generator*

Accuracy requirements are still under study.

2.3 *Pattern generator*

The jitter measuring circuit will normally be used with any suitable pattern generator providing the following facilities.

Note – When test signals are applied to the input of a digital demultiplexer, they must contain the frame alignment signal and justitication control bits. Other measurement techniques are available which do not require the addition of the frame alignment signal or justification control bits.

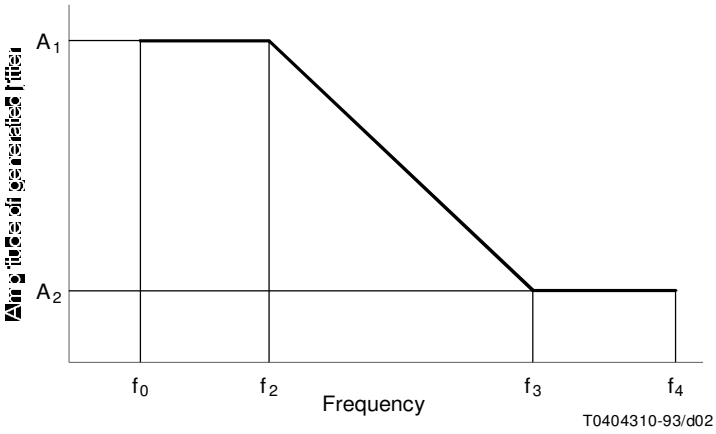

FIGURE 2/O.171

Generated jitter amplitude versus jitter frequency

TABLE 2/O.171

Generated jitter amplitude versus jitter frequency

Bit rate (kbit/s)	A_1: Minimum value of generated jitter from f_0 to f_2	A_2: Minimum value of generated jitter from f_3 to f_4
64	5.0 UI from 2 Hz to 600 Hz	0.5 UI from 6 kHz to 10 kHz
1 544	10.0 UI from 2 Hz to 200 Hz	0.5 UI from 4 kHz to 40 kHz
2 048	10.0 UI from 2 Hz to 2400 Hz	0.5 UI from 45 kHz to 100 kHz
6 312	10.0 UI from 2 Hz to 1600 Hz	0.5 UI from 32 kHz to 160 kHz
8 448	10.0 UI from 2 Hz to 400 Hz	0.5 UI from 8.5 kHz to 400 kHz
32 064	10.0 UI from 2 Hz to 1600 Hz	0.5 UI from 32 kHz to 800 kHz
34 368	10.0 UI from 2 Hz to 1000 Hz	0.5 UI from 20 kHz to 800 kHz
44 736	16.0 UI from 2 Hz to 3200 Hz	0.5 UI from 100 kHz to 4500 kHz
139 264	10.0 UI from 2 Hz to 500 Hz	0.5 UI from 10 kHz to 3500 kHz
8 448 (low Q)	10.0 UI from 2 Hz to 10.7 kHz	0.5 UI from 200 kHz to 400 kHz

Note 1 to Figure 2/O.171 and Table 2/O.171 – Amplitude of jitter specified as peak-to-peak value in unit intervals (UI).

Note 2 to Figure 2/O.171 and Table 2/O.171 – f_1 lies between f_0 and f_2 (see Figure 3/O.171 and Table 3/O.171). It is not defined here since it is not significant in the context of the requirements of the clock generator.

2.3.1 *Patterns*

The pattern generator shall be capable of providing the following patterns:

Note – Longer pseudo-random patterns may be necessary for jitter measurements on digital line systems and digital line sections (see Recommendation G.703 [1]).

2.3.1.1 For use at bit rates of 64 kbit/s, a pseudo-random pattern of $2^{11} - 1$ bit length corresponding to Recommendation O.152. Encoding in accordance with § 1.2.1 of Recommendation G.703 [1].

2.3.1.2 For use at bit rates of 1544 kbit/s 6312 kbit/s and 44 736 kbit/s, pseudo-random patterns of $2^{15} - 1$, $2^{20} - 1$, $2^{23} - 1$ bit length corresponding to § 2 of Recommendation O.151 [3].

Note – Definition of the $2^{20} - 1$ pseudo-random pattern is under study.

2.3.1.3 For use at bit rates of 2048 kbit/s, 8448 kbit/s and 32 064 kbit/s, a pseudo-random pattern of $2^{15} - 1$ length corresponding to § 2 of Recommendation O.151 [3].

2.3.1.4 For use at bit rates of 34 368 kbit/s and 139 264 kbit/s, a pseudo-random pattern of $2^{23} - 1$ bit length corresponding to § 2 of Recommendation O.151 [3].

2.3.1.5 For use at all bit rates, a 1000 1000 repetitive pattern.

2.3.1.6 As an option and for use at all bit rates:

a) two freely programmable 8-bit patterns capable of being alternated at a low rate (e.g. from 10 Hz to 100 Hz);

b) a freely programmable 16-bit pattern.

2.3.2 *Generation errors*

The detailed specification of pattern generator parameters, to be compatible with the jitter measuring circuit specification, is under study.

3 Jitter measuring circuit

3.1 *Input sensitivity*

The jitter measuring circuit is required to operate satisfactorily under the following input conditions:

a) The specification for equipment output ports listed in Recommendation G.703 [1].

b) The jitter measuring circuit shall also be capable of measuring at protected test points on digital equipment. Therefore, an additional gain of 30 dB (40 dB) shall be provided to compensate for the flat loss at the monitoring points already provided on some equipment.

Note 1 – As an option for instrumentation operating at an interface of 1544 kbit/s the additional gain, where provided, shall be 40 dB.

Note 2 – The influence of the additional gain of 40 dB and of frequency dependent cable loss on the measurement accuracy is under study.

3.2 *Measurement ranges*

3.2.1 The jitter measuring circuit shall be capable of measuring peak-to-peak jitter. The measurement ranges to be provided are to be optional but for reasons of compatibility the jitter amplitude/jitter frequency response of the jitter measuring circuit shall meet the requirements of Figure 3/O.171 and Table 3/O.171 where f_1 to f_4 are the frequencies defining the jitter frequencies to be measured.

3.2.2 When measuring peak-to-peak jitter it shall also be possible to count the number of occasions and the period of time for which a given selectable threshold of jitter is exceeded. It shall be possible to record these events by means of an external counter, or an internal counter as an option.

3.2.3 It shall be possible to set the threshold of § 3.2.2 at any selected measurement value within the measuring range of the jitter measuring circuit.

3.2.4 As an option, the jitter measuring circuit shall be capable of measuring r.m.s. jitter. In such cases it shall be possible to measure 3.0 unit intervals (UI) at jitter frequencies up to f_2, and 0.15 UI at jitter frequencies from f_3 to f_4 of Figure 3/O.171 and Table 3/O.171, the measurement ranges being optional.

3.2.5 Where the option in § 3.2.4 is not provided, the analogue output can be used to make r.m.s. measurements with an external meter.

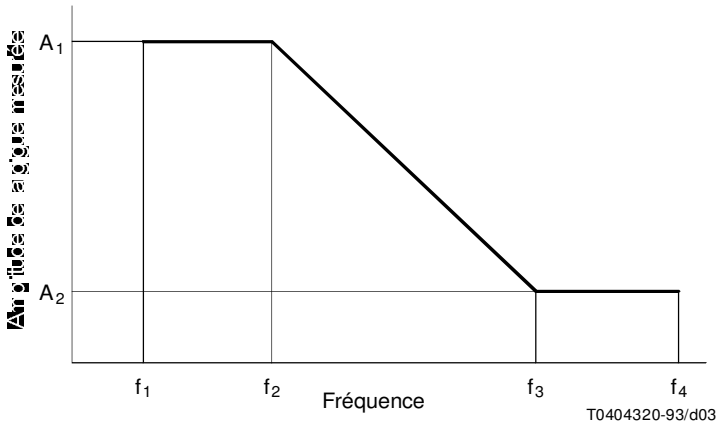

FIGURE 3/O.171

Amplitude de la gigue mesurée en fonction de la fréquence

TABLE 3/O.171

Measured jitter amplitude versus jitter frequency

Bit rate (kbit/s)	A_1: Maximum value of jitter to be measured f_1 to f_2	A_2: Maximum value of jitter to be measured f_3 to f_4
64	5.0 UI from 20 Hz to 600 Hz	0.5 UI from 6 kHz to 10 kHz
1 544	10.0 UI from 10 Hz to 200 Hz	0.3 UI from 7 kHz to 40 kHz
2 048	10.0 UI from 20 Hz to 2400 Hz	0.5 UI from 45 kHz to 100 kHz
6 312	10.0 UI from 10 Hz to 1600 Hz	0.5 UI from 32 kHz to 160 kHz
8 448	10.0 UI from 20 Hz to 400 Hz	0.5 UI from 8.5 kHz to 400 kHz
32 064	10.0 UI from 60 Hz to 1600 Hz	0.5 UI from 32 kHz to 800 kHz
34 368	10.0 UI from 100 Hz to 1000 Hz	0.5 UI from 20 kHz to 800 kHz
44 736	16.0 UI from 10 Hz to 3200 Hz	0.5 UI from 100 kHz to 4500 kHz
139 264	10.0 UI from 200 Hz to 500 Hz	0.5 UI from 10 kHz to 3500 kHz
8 448 (low Q)	10.0 UI from 20 Hz to 10.7 kHz	0.5 UI from 200 kHz to 400 kHz

Note to Figure 3/O.171 and Table 3/O.171 – Amplitude of jitter specified as peak-to-peak value in unit intervals (UI).

3.3 *Measurement bandwidths*

3.3.1 The basic jitter measuring circuit shall contain filters to limit the band of the jitter frequencies to be measured at the various bit rates. Additional filters shall be provided to further limit the bandwidth for the measurement of specified jitter spectra as defined in the G.700-series Recommendations and for other uses. These additional filters may be either internal or external to the jitter measuring circuit. The filters are to be connected between the phase detector and the measuring device. The bandwidth of the jitter measuring circuit and the filters shall be in accordance with Table 4/O.171.

TABLE 4/O.171

Jitter measurement bandwidths and highpass filter cutoff frequencies

Bit rate (kbit/s)	Jitter measurement bandwidth				3 dB-point of supplementary filters	
	f_0 (lower 3 dB point) (Hz)	f_1 (Hz)	f_4 (kHz)	f_5 (upper 3 dB point) (kHz)	Highpass filter No. 1	Highpass filter No. 2
64	2	20	10	≤ 20	20 Hz	3 kHz
1 544	2	10	40	≤ 80	10 Hz	8 kHz
2 048	2	20	100	≤ 200	20 Hz	700 Hz 18 kHz
6 312	2	10	160	≤ 320	10 Hz 60 Hz	24 kHz 32 kHz
8 448	2	20	400	≤ 800	20 Hz	3 kHz 80 kHz
32 064	2	60	800	≤ 1600	60 Hz	160 kHz
34 368	2	100	800	≤ 1600	100 Hz	10 kHz
44 736	2	10	4500	≤ 9000	10 Hz	900 kHz
139 264	2	200	3500	≤ 7000	200 Hz	10 kHz

Note 1 – The accuracy of the instrument is specified between frequencies f_1 and f_4.

Note 2 – Two values are specified for highpass filter No. 1 at 6312 kbit/s and highpass filter No. 2 at 2048 kbit/s, 6312 kbit/s and 8448 kbit/s.

3.3.2 *Frequency response of jitter measuring circuit and filters*

The response of all filters within the passband shall be such that the accuracy requirements of the jitter measuring circuit are met.

At frequencies below the lower 3-dB point, the attenuation of the highpass filtration shall rise with a value greater than, or equal to, 20 dB per decade.

At frequencies above the upper 3-dB point the attenuation of the lowpass filtration shall rise with a value greater than, or equal to, 60 dB per decade.

However, the maximum attenuation of the filters shall be at least 60 dB.

Note – The effect of nonsinusoidal jitter on the requirements for the filters is still under study.

3.4 *Measurement accuracy*

3.4.1 *General*

The measuring accuracy of the jitter measuring circuit is dependent upon several factors such as fixed intrinsic error, frequency response and pattern-depending error of the internal reference timing circuits. In addition there is an error which is a function of the actual reading.

The total error at 1-kHz jitter frequency (excluding the error due to frequency response) shall be less than

$$\pm 5\% \text{ of reading} \pm X \pm Y$$

where X is the fixed error of Table 5/O.171 and Y an error of 0.01 UI p-p (0.002 $UI_{r.m.s.}$) which applies if internal timing extraction is used.

3.4.2 *Fixed error*

For the system bit rates and for the indicated test sequences the fixed error of the jitter measuring circuit shall be as listed in Table 5/O.171 when measured at any jitter frequency between f_1 and f_4 of Figure 3/O.171.

TABLE 5/O.171

Fixed error in jitter measurements

Bit rate (kbit/s)	Jitter in UI for given patterns					
	1000 1000		Pseudo-random[a)]		All ones or clock input	
	p-p	r.m.s.	p-p	r.m.s.	p-p	r.m.s.
64	0.005	0.002	0.025	0.004	0.004	0.001
1 544	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
2 048	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
6 312	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
8 448	< 0.005	< 0.002	< 0.025	< 0.004	< 0.004	< 0.001
32 064	Under study					
34 368	< 0.025	< 0.01	< 0.055	< 0.015	< 0.02	< 0.01
44 736	Under study					
139 264	< 0.03	< 0.015	< 0.085	< 0.02	< 0.025	< 0.015

a) See § 2.3.1.

3.4.3 *Error at other frequencies*

At jitter frequencies between f_1 and f_4 other than 1 kHz, the error additional to that defined in § 3.4.1 shall be as listed in Table 6/O.171.

Note – The limits of measuring accuracy of the jitter measuring circuit given in § 3.4 are provisional and are still under study.

TABLE 6/O.171

Frequency response error

Bit rate (kbit/s)	Measurement bandwidth		Additional error referring to error at 1 kHz
	f_1 (Hz)	f_4 (kHz)	
64	20	10	± 2% 20 Hz to 600 Hz ± 3% 600 Hz to 10 kHz
1 544	10	40	± 4% f_1 to 1 kHz; ± 2% to f_4
2048	20	100	± 2% f_1 to f_4
6 312	10	160	± 4% f_1 to 1 kHz; ± 2% to f_4
8 448	20	400	± 2% f_1 to 300 kHz ± 3% 300 Hz to f_4
32 064	60	800	± 2% 60 Hz to 300 kHz
34 368	100	800	± 3% 300 kHz to f_4
44 736	10	4500	± 4% 10 Hz to 200 Hz ± 2% 200 Hz to 300 kHz ± 3% 300 kHz to 1 MHz
139 264	200	3500	± 5% 1 MHz to 3 MHz ± 10% > 3 MHz

Note – The accuracy requirements of this table can be met when periodic test patterns with low zero content or clock signals are used to perform the jitter measurement. When using pseudo-random or random sequences, larger measurement errors have to be expected.

3.5 *Additional facilities*

3.5.1 *Analogue output*

The jitter measuring circuit shall provide an analogue output signal to enable measurements to be made externally to the jitter measuring circuit.

3.5.2 *Reference timing signal*

A reference timing signal for the phase detector is required. For end-to-end measurements it may be derived in the jitter measuring circuit from any input pattern. For loop-measurements it may be derived from a suitable clock source.

4 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in § 2.1 of Recommendation O.3 [4].

References

[1] CCITT Recommendation G.703 *Physical/electrical characteristics of hierarchical digital interfaces*.

[2] CCITT Recommendation G.823 *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[3] CCITT Recommendation O.151 *Error performance measuring equipment operating at the primary rate and above*.

[4] CCITT Recommendation O.3 *Climatic conditions and relevants tests for measuring equipment*.