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SPECIFICATIONS OF MEASURING EQUIPMENT

ERROR PERFORMANCE MEASURING EQUIPMENT FOR BIT RATES OF 64 kbit/s AND $N \times 64$ kbit/s

Recommendation O.152

FOREWORD

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CCITT NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized private operating agency.

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Recommendation O.152

ERROR PERFORMANCE MEASURING EQUIPMENT FOR BIT RATES OF 64 kbit/s AND $N \times 64$ kbit/s

(Published 1984; revised 1988, 1992)

Abstract

Defines the requirements for an equipment to measure bit-error performance at 64 kbit/s and $N \times 64$ kbit/s.

Keywords

– digital error detector;

– digital pattern generator;

– error performance measurement;

– measurement;

– tester.

PREAMBLE

The requirements for the characteristics of a bit-error performance measuring equipment which are described below must be adhered to in order to ensure compatibility between equipment produced by different manufacturers.

1 General

The equipment is designed to measure the bit-error performance of digital paths (operating at 64 kbit/s and $N \times 64$ kbit/s) by the direct comparison of a pseudo-random test pattern with locally generated test pattern identical to the transmitted test pattern.

2 Test patterns

The following patterns are recommended (see Recommendation O.150 [8], for further details).

2.1 *Pseudo-random pattern of $2^{11} - 1$ (2047 bit) pattern length*

This pattern is primarily intended for error and jitter measurements on circuits operating at bit rates of 64 kbit/s and $N \times 64$ kbit/s.

The pattern may be generated in an eleven-stage shift register whose 9th and 11th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

Number of shift register stages	11
Length of pseudo-random sequence	$2^{11} - 1 = 2047$ bits
Longest sequence of ZEROs	10 (non-inverted signal)

Note 1 – In the case of international testing where the measurement includes systems based on 1544 kbit/s, it is necessary to modify the test sequence in such a way that more than seven consecutive ZEROs are avoided. This is achieved by forcing the output bit to ONE whenever the previous 7 bits of the sequence are all ZEROs.

Note 2 – It is recommended to use the test pattern of 2047 bit length also at other bit rates in the range of 48 kbit/s to 168 kbit/s.

Note 3 – When performing measurements at a bit rate of $N \times 64$ kbit/s, consecutive 8-bit blocks of the test pattern shall be transmitted in consecutive time slots. In this case, the beginning of the test pattern need not to be related to the beginning of a frame.

Note 4 – Whether *N* can be any number between 1 and 31 requires further study.

2.2 *Fixed patterns (optional)*

Fixed patterns of all ONEs (...1111...) and alternating ONEs and ZEROs (...1010...) may be provided.

2.3 *Loss of sequence synchronization*

Sequence synchronization shall be considered to be lost and resynchronization shall be started if:

a) the bit-error ratio is ≥ 0.2 during an integration interval of 1 second; or

b) it can be unambiguously identified that the test pattern and the reference pattern are out of phase.

Note – One method to recognize the out-of-phase condition is the evaluation of the error pattern resulting from the bit-by-bit comparison. If the error pattern has the same structure as the pseudo-random test pattern, then the out-of-phase condition can be recognized.

This sub-section requires further study.

3 Bit rate

Bit rate in accordance with § 1 of Recommendation G.703 [1] and Recommendation V.36 [2] of 64 kbit/s:

a) bit rate tolerance (Recommendation G.703 [1]): $\pm 100 \cdot 10^{-6}$,

b) bit rate tolerance (Recommendation V.36 [2]), optional: $\pm 50 \cdot 10^{-6}$.

4 Interfaces

The interface characteristics (impedances, levels, codes, etc.) should be in accordance with Recommendations G.703 [1], I.430 [7] (optional) and V.11 [3] (optional).

In addition to providing for terminated measurements, the measuring set shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance and/or additional gain must be provided to compensate for the loss at monitoring points already provided on some equipments.

4.1 *Interfaces corresponding to Recommendation G.703* [1]

Three interfaces shall be provided:

a) a codirectional interface in accordance with § 1.2.1 of Recommendation G.703 [1];

b) a centralized clock interface in accordance with § 1.2.2 of Recommendation G.703 [1];

c) a contradirectional interface in accordance with § 1.2.3 of Recommendation G.703 [1].

4.2 *Method of clock synchronization*

The following modes of synchronization shall be selectable:

a) Lock the digital generator clock rate to that at the input of the receive side of the measuring set (for the codirectional interface).

b) Allow the generator clock to free run within the overall allowed frequency tolerances.

c) Lock the digital generator clock rate to an external clock signal. (Configuration of input for external clock in accordance with Recommendation G.703 [1].)

4.3 *Interface corresponding to Recommendation I.430* [7]

For further study. This study should include means for obtaining access to the individual 64 kbit/s channels at the S and T interface points.

4.4 *Interface corresponding to Recommendation V.11* [3]

As an option, an interface in accordance with Recommendation V.11 [3] shall be provided.

5 Bit-error ratio measuring range

The receiving equipment of the set should be capable of measuring bit-error ratios in the range 10^{-2} to 10^{-7}. The measurement time should be sufficiently long to achieve accurate measurements. In addition, it should be possible to measure bit-error ratios smaller than 10^{-7}. This can be achieved by providing the capability to count cumulative errors.

6 Block-error ratio measurements

Optionally, the instrument should be capable of performing block-error measurements in addition to the bit-error measurements. If provided, it should be possible to measure block-error ratios in the range 10^{0} to 10^{-5} when using the pseudo-random test pattern with a block length of 2047 bits.

7 Mode of operation

The mode of operation should be such that the signal to be tested is first converted into a unipolar (binary) signal in the error measuring instrument and subsequently the bit comparison is made also with a reference signal in binary form.

8 Error evaluation

8.1 *Measurement of errored time intervals*

The instrument shall be capable of detecting errored seconds and other errored or error-free time intervals as defined by Recommendation G.821 [4]. The number of errored or error-free time intervals in a selectable observation period from 1 minute to 24 hours, or continuous, shall be counted and displayed.

For this measurement, the error detection circuits of the instrument shall be controlled by an internal timer which sets intervals of equal length and which operates independently of the occurrence of errors.

8.2 *Measurement of short-term mean error ratio*

8.2.1 It shall be possible to record the time intervals as defined in Recommendation G.821 [4], during which the bit-error ratio is less than $1 \cdot 10^{-6}$.

8.2.2 It shall be possible to record the one-second intervals during which the bit-error ratio is less than $1 \cdot 10^{-3}$.

9 Recording of measurement results

As an option an interface shall be provided which allows connecting external equipment for further processing the measuring results.

The interface shall comply with Recommendation V.24 [5] or the interface bus according to IEC Publication 625 [6].

10 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in § 2.1 of Recommendation O.3 [9].

References

[1] CCITT Recommendation G.703 – *Physical/electrical characteristics of hierarchical digital interfaces.*

[2] CCITT Recommendation V.36 – *Modems for synchronous data transmission using 60-108 kHz group band circuits.*

[3] CCITT Recommendation V.11 – *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications.*

[4] CCITT Recommendation G.821 – *Error performance on an international digital connection forming part of an integrated services digital network.*

[5] CCITT Recommendation V.24 – *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment.*

[6] IEC Publication 625 – *An Interface system for programmable measuring instruments (byte serial, bit parallel).*

[7] CCITT Recommendation I.430 – *Basic user-network interface-Layer/Specification.*

[8] CCITT Recommendation O.150 – *Digital test patterns for performance measurements on digital transmission equipment.*

[9] CCITT Recommendation O.3 – *Climatic conditions and relevant tests for measuring equipment.*