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SPECIFICATIONS OF MEASURING EQUIPMENT

DIGITAL TEST PATTERNS FOR PERFORMANCE MEASUREMENTS ON DIGITAL TRANSMISSION EQUIPMENT

Recommendation O.150

FOREWORD

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Recommendation O.150 was prepared by Study Group IV and was approved under the Resolution No. 2 procedure on the 5th of October 1992.

CCITT NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized private operating agency.

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Recommendation O.150

DIGITAL TEST PATTERNS FOR PERFORMANCE MEASUREMENTS ON DIGITAL TRANSMISSION EQUIPMENT

(1992)

Abstract

Defines all digital test patterns referenced in the O-Series Recommendations.

Keywords

— digital test patterns;

— measurement;

— pseudo-random test patterns;

— tester.

1 Introduction

This Recommendation contains a summary of the various digital test patterns specified in the O-Series Recommendations. It is intended to be a help in finding the right patterns for different applications.

2 Need for standardized test patterns

Bit error measurements are an important means to assess the performance of digital transmission equipment. So-called "true" bit error measurements, during which every error can be detected, can only be carried out if the bit sequence of the pattern used for the measurement is completely known. Because of its random nature, this condition is normally not fulfilled by real traffic.

Therefore, it is necessary to specify reproducible test patterns which simulate real traffic as closely as possible. Reproducible test patterns are also a prerequisite to perform end-to-end measurements.

Pseudo-random sequences are the most common answer to this problem. In addition to strings of n consecutive ZEROs (so-called inverted signal) and n — 1 consecutive ONEs, such patterns contain any possible combination of ZEROs and ONEs within a string length depending on n. For the value of n, see § 3.

Pseudo-random sequences of various lengths have been specified by the CCITT.

3 Properties of pseudo-random test patterns

The properties of a test pattern should meet the requirements of the system under test. In general, the length of a pseudo-random sequence shall increase with the bit rate at which measurements are performed. This avoids having a pattern repetition frequency which is too high and which would not be in accordance with the situation found in practice.

Pseudo-random sequences may be produced by means of shift registers with appropriate feedback. If the shift register has n stages, the maximum pattern length will be 2^n — 1 bits.

If the digital signal is taken directly from the output of the shift register (non-inverted signal) the longest string of consecutive ZEROs will equal n — 1. If the signal is inverted, n consecutive ZEROs will be produced.

It is possible to generate pseudo-random sequences with these properties by means other than shift registers.

3.1 *Error measurements through scramblers*

The unit under test may contain scramblers. This may yield unexpected measurement results if the value *n* as described in § 3 has common integer multiples with the number of stages of the scrambler. To reduce the probability of occurrence of this problem, the values of *n* for test patterns recently specified are prime numbers.

3.2 *Loss of sequence synchronization*

Bit error measurements using pseudo-random sequences can only be performed if the reference pattern produced on the receiving side of the test set-up is correctly synchronized to the pattern coming from the object under test. In order to achieve compatible measurement results, it is necessary that the sequence synchronization characteristics are specified.

The following requirement is applicable to all O-Series Recommendations dealing with error performance measurements using pseudo-random sequences.

Sequence synchronization shall be considered to be lost and resynchronization shall be started if

a) the bit error ratio is ≥ 0.20 during an integration interval of 1 second; or

b) it can be unambiguously identified that the test pattern and the reference pattern are out of phase.

Note — One method to recognize the out-of-phase condition is the evaluation of the error pattern resulting from a bit-by-bit comparison. If the error pattern has the same structure as the pseudo-random test pattern, then the out-of-phase condition can be recognized.

This sub-section requires further study.

3.3 *"Framed" measurements*

Certain measurements require that the test pattern is transmitted as "payload" within a valid frame.

In this case the transmission of the test patterns shall be stopped while the framing bits are transmitted.

3.4 *Jitter measurements*

Digital test patterns are not only used in error measurements but also for measuring the jitter transfer function or tolerable input jitter. Special attention should be paid in this case to the length of the test pattern used in the measurement. If the pattern is too short (high pattern repetition frequency), the spectral distribution of the test signal may differ substantially from the properties of real traffic. In this case, the measurement results will not reflect the practical situation. See Annex A to Recommendation G.823 [1].

4 Digital test patterns defined in the O-Series Recommendations

This section describes the digital test patterns defined in the O-Series Recommendations and their main applications. Table 1/O.150 gives a summary.

TABLE 1/O.150

Digital test patterns defined in the O-Series Recommendations

Length of pattern (bits)	Consecutive zeros	Reference	Use of pattern
$2^9 - 1$	8	O.153	Error measurements on data circuits at bit rates up to 14 400 bit/s
$2^{11} - 1$	10	O.152	Error and jitter measurements at bit rates of 64 kbit/s and $N \times 64$ kbit/s
$2^{15} - 1$	15	O.151	Error and jitter measurements at bit rates of 1544, 2048, 6312, 8448, 32 064 and 44 736 kbit/s
$2^{20} - 1$	19	O.153	Error measurements on data circuits at bit rates up to 72 kbit/s
$2^{20} - 1$	14	O.151	Error and jitter measurements at bit rates of 1544, 6312, 32 064 and 44 736 kbit/s
$2^{23} - 1$	23	O.151	Error and jitter measurements at bit rates of 34 368 and 139 264 kbit/ss

4.1 *511-bit pseudo-random test pattern*

This pattern is primarily intended for error measurements on data circuits at bit rates up to 14 400 bit/s (see Recommendation O.153).

The pattern may be generated in a nine-stage shift register whose 5th and 9th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. The pattern begins with the first ONE of 9 consecutive ONEs.

— Number of shift register stages 9

— Length of pseudo-random sequence $2^9 - 1 = 511$ bits

— Longest sequence of ZEROs 8 (non-inverted signal)

4.2 *2047-bit pseudo-random test pattern*

This pattern is primarily intended for error and jitter measurements on circuits operating at bit rates of 64 kbit/s and $N \times 64$ kbit/s (see Recommendations O.152 and O.153).

The pattern may be generated in an eleven-stage shift register whose 9th and 11th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

— Number of shift register stages 11

— Length of pseudo-random sequence $2^{11} - 1 = 2047$ bits

— Longest sequence of ZEROs 10 (non-inverted signal)

Note 1 — When performing measurements at a bit rate of $N \times 64$ kbit/s, consecutive 8-bit-blocks of the test pattern shall be transmitted in consecutive time slots. The beginning of the pseudo-random test pattern need not be related to the frame repetition rate.

Note 2 — Whether N can be any number between 1 and 31 requires further study.

4.3 *32 767-bit pseudo-random test pattern*

This pattern is primarily intended for error and jitter measurements at bit rates of 1544, 2048, 6312, 8448, 32 064 and 44 736 kbit/s (see Recommendation O.151).

The pattern may be generated in a fifteen-stage shift register whose 14th and 15th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

— Number of shift register stages 15

— Length of pseudo-random sequence $2^{15} - 1 = 32\,767$ bits

— Longest sequence of ZEROs 15 (inverted signal)

4.4 *1 048 575-bit pseudo-random test pattern*

This pattern is primarily intended for error measurements on data circuits at bit rates up to 72 kbit/s (see Recommendation O.153).

The pattern may be generated in a twenty-stage shift register whose 3rd and 20th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

— Number of shift register stages 20

— Length of pseudo-random sequence $2^{20} - 1 = 1\,048\,575$ bits

— Longest sequence of ZEROs 19 (non-inverted signal)

Note — The two test patterns of length $2^{20} - 1$ bits described in §§ 4.4 and 4.5 are not identical because different feedback mechanisms are used when the patterns are produced by shift registers. The pattern specified in § 4.5 suppresses consecutive sequences of more than 14 ZEROs.

4.5 *1 048 575-bit pseudo-random test pattern*

This pattern is primarily intended for error and jitter measurements at bit rates of 1544, 6312, 32 064 and 44 736 kbit/s (see Recommendation O.151).

The pattern may be generated in a twenty-stage shift register whose 17th and 20th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage. An output bit is forced to be a ONE whenever the previous 14 bits are all ZERO.

— Number of shift register stages 20

— Length of pseudo-random sequence $2^{20} - 1 = 1\,048\,575$ bits

— Longest sequence of ZEROs 15 (see Note)

This pseudo-random sequence satisfies the following:

$$Q_{n+1}(k+1) = Q_n(k),\ n = 1, 2, ..., 19,$$

$$Q_1(k+1) = Q_{17}(k) \oplus Q_{20}(k), \text{ and}$$

$$RD(k) = Q_{20}(k) + \overline{Q_6(k) + ... + Q_{19}(k)}$$

where:

$Q_n(k)$ is the present state of nth stage,

$Q_n(k+1)$ is the next state of nth stage,

$RD(k)$ is the present value of output,

$+$ is a logic OR operation,

$\oplus$ is a logic EXCLUSIVE OR operation,

$\overline{\ \ }$ is a logic NEGATION operation.

Note — The two test patterns of length 2^{20} — 1 bits described in §§ 4.4 and 4.5 are not identical because different feedback mechanisms are used when the patterns are produced by shift registers. The pattern specified in this sub-section suppresses consecutive sequences of more than 14 ZEROs.

4.6 *8 388 607-bit pseudo-random test pattern*

This pattern is primarily intended for error and jitter measurements at bit rates of 34 368 and 139 264 kbit/s (see Recommendation O.151).

The pattern may be generated in a twenty-three-stage shift register whose 18th and 23rd stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

— Number of shift register stages 23

— Length of pseudo-random sequence 2^{23} — 1 = 8 388 607 bits

— Longest sequence of ZEROs 23 (inverted signal)

References

[1] CCITT Recommendation G.823 *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.*