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ISDN USER-NETWORK INTERFACES

BASIC USER-NETWORK INTERFACE – LAYER 1 SPECIFICATION

ITU-T Recommendation I.430

(Previously “CCITT Recommendation”)

FOREWORD

The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the International Telecommunication Union. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, established the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

ITU-T Recommendation I.430 was revisd by the ITU-T Study Group XVIII (1988-1993) and was approved by the WTSC (Helsinki, March 1-12, 1993).

NOTES

1 As a consequence of a reform process within the International Telecommunication Union (ITU), the CCITT ceased to exist as of 28 February 1993. In its place, the ITU Telecommunication Standardization Sector (ITU-T) was created as of 1 March 1993. Similarly, in this reform process, the CCIR and the IFRB have been replaced by the Radiocommunication Sector.

In order not to delay publication of this Recommendation, no change has been made in the text to references containing the acronyms "CCITT, CCIR or IFRB" or their associated entities such as Plenary Assembly, Secretariat, etc. Future editions of this Recommendation will contain the proper terminology related to the new ITU structure.

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Recommendation I.430

BASIC USER-NETWORK INTERFACE – LAYER 1 SPECIFICATION

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988 and at Helsinki 1993)

1 General

This Recommendation defines the layer 1 characteristics of the user-network interface to be applied at the S or T reference points for the basic interface structure defined in Recommendation I.412. The reference configuration for the interface is defined in Recommendation I.411 and is reproduced in Figure 1.

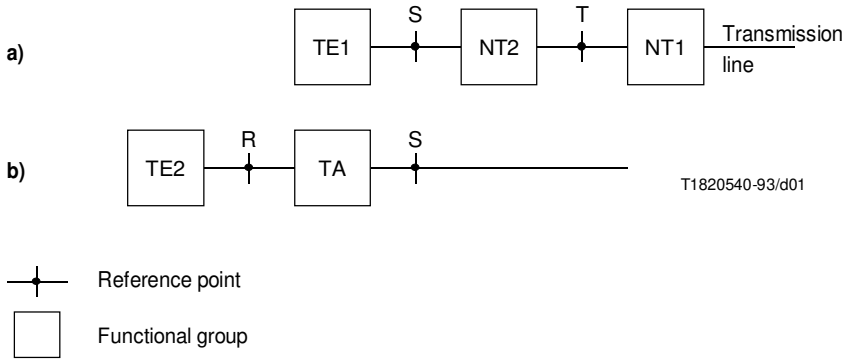


FIGURE 1/I.430

Reference configurations for the ISDN user-network interfaces

In this Recommendation, the term "NT" is used to indicate network terminating layer 1 aspects of NT1 and NT2 functional groups, and the term "TE" is used to indicate terminal terminating layer 1 aspects of TE1, TA and NT2 functional groups, unless otherwise indicated. However, in 6.2 only, the terms "NT" and "TE" have the following meaning: the term "NT" is used to indicate the layer 1 network side of the basic access interface; the term "TE" is used to indicate the layer 1 terminal side of the basic access interface.

Terms used in this Recommendation, together with their definitions, are contained in Recommendation I.112.

2 Service characteristics

2.1 Services required from the physical medium

Layer 1 of this interface requires a balanced metallic transmission medium, for each direction of transmission, capable of supporting 192 kbit/s.

2.2 Service provided to layer 2

Layer 1 provides the following services to layer 2 and the management entity.

2.2.1 Transmission capability

Layer 1 provides the transmission capability, by means of appropriately encoded bit streams, for the B- and D-channels and the related timing and synchronization functions.

2.2.2 Activation/deactivation

Layer 1 provides the signalling capability and the necessary procedures to enable customer TEs and/or NTs to be deactivated when required and reactivated when required. The activation and deactivation procedures are defined in 6.2.

2.2.3 D-channel access

Layer 1 provides the signalling capability and the necessary procedures to allow TEs to gain access to the common resource of the D-channel in an orderly fashion while meeting the performance requirements of the D-channel signalling system. These D-channel access control procedures are defined in 6.1.

2.2.4 Maintenance

Layer 1 provides the signalling capability, procedures and necessary functions at layer 1 to enable maintenance functions to be performed.

2.2.5 Status indication

Layer 1 provides an indication to the higher layers of the status of layer 1.

2.3 Primitives between layer 1 and the other entities

Primitives represent, in an abstract way, the logical exchange of information and control between layer 1 and other entities. They neither specify nor constrain the implementation of entities or interfaces.

The primitives to be passed across the layer 1/2 boundary or to the management entity and parameter values associated with these primitives are defined and summarized in Table 1. For description of the syntax and use of the primitives, refer to Recommendation X.211 and relevant detailed descriptions in 6.

TABLE 1/I.430

Primitives associated with layer 1

Generic	Specific name		Parameter		Message unit content
	Request	Indication	Priority indicator	Message unit	
L1 ↔ L2					
PH-DATA	X (Note 1)	X	X (Note 2)	X	Layer 2 peer-to-peer message
PH-ACTIVATE	X	X	–	–	
PH-DEACTIVATE	–	X	–	–	
M ↔ L1					
MPH-ERROR	–	X	–	X	Type of error or recovery from a previously reported error
MPH-ACTIVATE	–	X	–	–	
MPH-DEACTIVATE	X	X	–	–	
MPH-INFORMATION	–	X	–	X	Connected/disconnected

NOTES

1 PH-DATA request implies underlying negotiation between layer 1 and layer 2 for the acceptance of the data.

2 Priority indication applies only to the request type.

3 Modes of operation

Both point-to-point and point-to-multipoint modes of operation, as described below, are intended to be accommodated by the layer 1 characteristics of the user-network interface. In this Recommendation, the modes of operation apply only to the layer 1 procedural characteristics of the interface and do not imply any constraints on modes of operation at higher layers.

3.1 Point-to-point operation

Point-to-point operation at layer 1 implies that only one source (transmitter) and one sink (receiver) are active at any one time in each direction of transmission at an S- or T-reference point. (Such operation is independent of the number of interfaces which may be provided on a particular wiring configuration – see 4).

3.2 Point-to-multipoint operation

Point-to-multipoint operation at layer 1 allows more than one TE (source and sink pair) to be simultaneously active at an S- or T- reference point. (The multipoint mode of operation may be accommodated, as discussed in 4, with point-to-point or point-to-multipoint wiring configurations.)

4 Types of wiring configuration

The electrical characteristics of the user-network interface are determined on the basis of certain assumptions about the various wiring configurations which may exist in the user premises. These assumptions are identified in two major configuration descriptions, 4.1 and 4.2, together with additional material contained in Annex A. Figure 2 shows a general reference configuration for wiring in the user premises.

4.1 Point-to-point configuration

A point-to-point wiring configuration implies that only one source (transmitter) and one sink (receiver) are interconnected on an interchange circuit.

4.2 Point-to-multipoint configuration

A point-to-multipoint wiring configuration allows more than one source to be connected to the same sink or more than one sink to be connected to the same source on an interchange circuit. Such distribution systems are characterized by the fact that they contain no active logic elements performing functions (other than possibly amplification or regeneration of the signal).

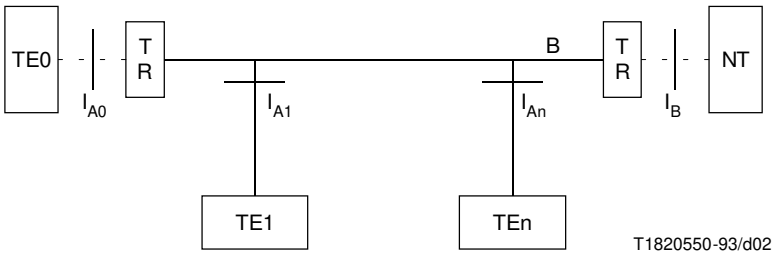
4.3 Wiring polarity integrity

For a point-to-point wiring configuration, the two wires of the interchange circuit pair may be reversed. However, for point-to-multipoint wiring configuration, the wiring polarity integrity of the interchange circuit (TE-to-NT direction) must be maintained between TEs (see the reference configuration in Figure 21).

In addition, the wires of the optional pairs, which may be provided for powering, may not be reversed in either configuration.

4.4 Location of the interfaces

The wiring in the user premises is considered to be one continuous cable run with jacks for the TEs and NT attached directly to the cable or using stubs less than 1 metre in length. The jacks are located at interface points I_A and I_B (see Figure 2). One interface point, I_A, is adjacent to each TE. The other interface point I_B, is adjacent to the NT. However, in some applications, the NT may be connected to the wiring without the use of a jack or with a jack which accommodates multiple interfaces (e.g. when the NT is a port on a PBX). The required electrical characteristics (described in 8) for I_A and I_B are different in some aspects.



TR Terminating resistor
I Electrical Interface
B Location of I_B when the terminating resistor (TR) is included in the NT

FIGURE 2/I.430

Reference configuration for wiring in the user premises location

4.5 NT and TE associated wiring

The wiring from the TE or the NT to its appropriate jack affects the interface electrical characteristics. A TE, or an NT that is not permanently connected to the interface wiring, may be equipped with either of the following for connection to the interface point (I_A and I_B, respectively):

- a hard wired connecting cord (of not more than 10 metres in the case of a TE, and not more than 3 metres in the case of an NT) and a suitable plug; or
- a jack with a connecting cord (of not more than 10 metres in the case of a TE, and not more than 3 metres in the case of an NT) which has a suitable plug at each end.

Normally, the requirements of this Recommendation apply to the interface point (I_A and I_B, respectively), and the cord forms part of the associated TE or NT. However, as a national option, where the terminating resistors are connected internally to the NT, the connecting cord may be considered as an integral part of the interface wiring. In this case, the requirements of this Recommendation may be applied to the NT at the connection of the connecting cord to the NT. Note that the NT may attach directly to the interface wiring without a detachable cord. Also note that the connector, plug and jack used for the connection of the detachable cord to the NT is subject to standardization. (Refer to 10.)

Although a TE may be provided with a cord of less than 5 metres in length, it shall meet the requirements of this Recommendation with a cord having a minimum length of 5 metres. As specified above, the TE cord may be detachable. Such a cord may be provided as a part of the TE, or the TE may be designed to conform to the electrical characteristics specified in 8 with a standard ISDN basic access TE cord conforming to the requirements specified in 8.9 of this Recommendation and having the maximum permitted capacitance.

The use of an extension cord, of up to 25 metres in length, with a TE is permitted but only on point-to-point wiring configurations. (The total attenuation of the wiring and of the cord in this case should not exceed 6 dB.)

5 Functional characteristics

The following subclauses show the functions for the interface.

5.1 Interface functions

5.1.1 B-channel

This function provides, for each direction of transmission, two independent 64 kbit/s channels for use as B-channels (as defined in Recommendation I.412).

5.1.2 Bit timing

This function provides bit (signal element) timing at 192 kbit/s to enable the TE and NT to recover information from the aggregate bit stream.

5.1.3 Octet timing

This function provides 8 kHz octet timing for the NT and TE.

5.1.4 Frame alignment

This function provides information to enable NT and TE to recover the time division multiplexed channels.

5.1.5 D-channel

This function provides, for each direction of transmission, one D-channel at a bit rate of 16 kbit/s, as defined in Recommendation I.412.

5.1.6 D-channel access procedure

This function is specified to enable TEs to gain access to the common resource of the D-channel in an orderly controlled fashion. The functions necessary for these procedures include an echoed D-channel at a bit rate of 16 kbit/s in the direction NT to TE. For the definition of the procedures relating to D-channel access see 6.1.

5.1.7 Power feeding

This function provides for the capability to transfer power across the interface. The direction of power transfer depends on the application. In a typical application, it may be desirable to provide for power transfer from the NT towards the TEs in order to, for example, maintain a basic telephony service in the event of failure of the locally provided power. (In some applications unidirectional power feeding or no power feeding at all, across the interface, may apply.) The detailed specification of power feeding capability is contained in 9.

5.1.8 Deactivation

This function is specified in order to permit the TE and NT to be placed in a low power consumption mode when no calls are in progress. For TEs that are power fed across the interface from power source 1 and for remotely power fed NTs, deactivation places the functions that are so powered into a low power consumption mode (see 9). The procedures and precise conditions under which deactivation takes place are specified in 6.2. (For some applications it will be appropriate for NTs to remain in the active state all the time.)

5.1.9 Activation

This function restores all the functions of a TE or an NT, which may have been placed into a lower power consumption mode during deactivation, to an operating power mode (see 9), whether under normal or restricted conditions. The procedures and precise conditions under which activation takes place are defined in 6.2. (For some applications it will be appropriate for NTs to remain in the active state all the time.)

5.2 Interchange circuits

Two interchange circuits, one for each direction of transmission, shall be used to transfer digital signals across the interface. All of the functions described in 5.1, except for power feeding, shall be carried by means of a digitally multiplexed signal structured as defined in 5.4.

5.3 Connected/disconnected indication

The appearance/disappearance of power is the criterion used by a TE to determine whether it is connected/disconnected at the interface. This is necessary for terminal endpoint identifier TEI assignments according to the procedures described in Recommendation I.441.

A TE which considers itself connected, when unplugged, can cause duplication of TEI values after reconnection. When duplication occurs, procedures described in Recommendation I.441 will permit recovery.

5.3.1 TEs powered across the interface

A TE which is powered from power source 1 or 2 across the interface shall use the detection of power source 1 or 2, respectively, to establish the connection status. (See 9 and Figure 21 for a description of the power sources.)

5.3.2 TEs not powered across the interface

A TE which is not powered across the interface may use either

a) the detection of power source 1 or 2, whichever may be provided, to establish the connection status; or

b) the presence/absence of local power to establish the connection status.

TEs which are not powered across the interface and are unable to detect the presence of power source 1 and 2 shall consider themselves connected/disconnected when local power is applied/removed.

NOTE – It is desirable to use the detection of power source 1 or 2 to establish the connection status when automatic TEI selection procedures are used within the management entity.

5.3.3 Indication of connection status

TEs shall inform the management entity of their connection/disconnection status (for TEI purposes) using :

a) MPH-INFORMATION indication (connected)

b) MPH-INFORMATION indication (disconnected)

5.4 Frame structure

In both directions of transmission, the bits shall be grouped into frames of 48 bits each. The frame structure shall be identical for all configurations (point-to-point and point-to-multipoint).

5.4.1 Bit rate

The nominal transmitted bit rate at the interfaces shall be 192 kbit/s in both directions of transmission.

5.4.2 Binary organization of the frame

The frame structures are different for each direction of transmission. Both structures are illustrated diagrammatically in Figure 3.

5.4.2.1 TE to NT

Each frame consists of the groups of bits shown in Table 2; each individual group is d.c.-balanced by its last bit (L bit).

5.4.2.2 NT to TE

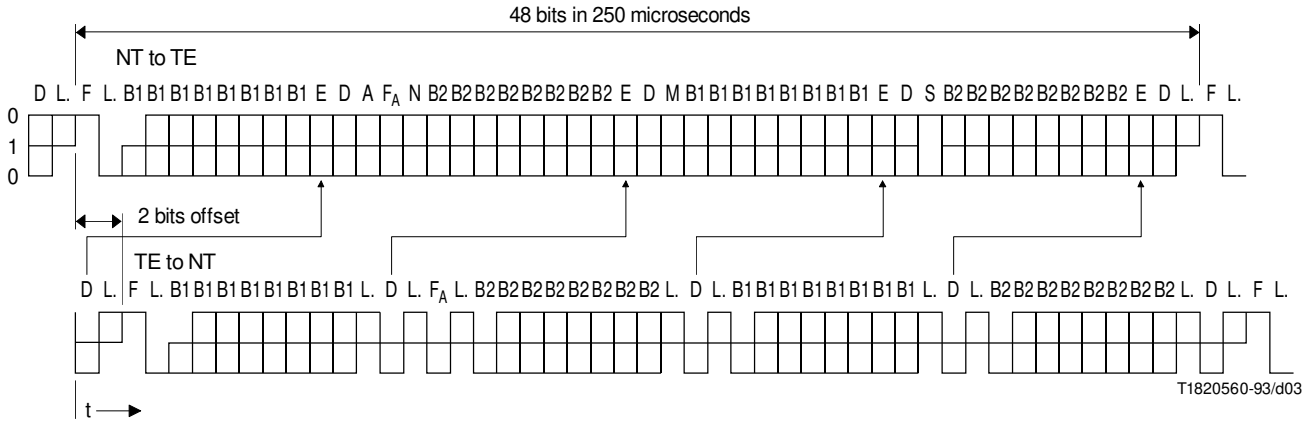
Frames transmitted by the NT contain an echo channel (E bits) used to retransmit the D bits received from the TEs. The D-echo channel is used for D-channel access control. The last bit of the frame (L bit) is used for balancing each complete frame.

The bits are grouped as shown in Table 3.

5.4.2.3 Relative bit positions

At the TEs, timing in the direction TE to NT shall be derived from the frames received from the NT.

The first bit of each frame transmitted from a TE towards the NT shall be delayed, nominally, by two bit periods with respect to the first bit of the frame received from the NT. Figure 3 illustrates the relative bit positions for both transmitted and received frames.



F	Framing bit	N	Bit set to a binary value N = $\overline{F}_A$ (NT to TE)
L	D.c. balancing bit	B1	Bit within B-channel 1
D	D-channel bit	B2	Bit within B-channel 2
E	D-echo-channel bit	A	Bit used for activation
F_A	Auxiliary framing bit (see 6.3)	S	Bit used for S-channel
		M	Multiframing bit

NOTES

1 Dots demarcate those parts of the frame that are independently d.c.-balanced.

2 The F_A bit in the direction TE to NT is used as a Q bit in every fifth frame if the Q-channel capability is applied (see 6.3.3).

3 The nominal 2-bit offset is as seen from the TE (I_A in Figure 2). The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration.

FIGURE 3/I.430

Frame structure at reference points S and T

TABLE 2/I.430

Bit position	Group
1 and 2	Framing signal with balance bit
3 to 11	B1-channel (first octet) with balance bit
12 and 13	D-channel bit with balance bit
14 and 15	F_A auxiliary framing bit for Q bit with balance bit
16 to 24	B2-channel (first octet) with balance bit
25 and 26	D-channel bit with balance bit
27 to 35	B1-channel (second octet) with balance bit
36 and 37	D-channel bit with balance bit
38 to 46	B2-channel (second octet) with balance bit
47 and 48	D-channel bit with balance bit

TABLE 3/I.430

Bit position	Group
1 and 2	Framing signal with balance bit
3 to 10	B1-channel (first octet)
11	E-, D-echo channel bit
12	D-channel bit
13	Bit A used for activation
14	F_A auxiliary framing bit
15	N bit (coded as defined in 6.3)
16 to 23	B2-channel (first octet)
24	E-, D-echo channel bit
25	D-channel bit
26	M, multiframing bit
27 to 34	B1-channel (second octet)
35	E-, D-echo channel bit
36	D-channel bit
37	S
38 to 45	B2-channel (second octet)
46	E-, D-echo channel bit
47	D-channel bit
48	Frame balance bit
NOTE – The use of the S bit is optional, and when not used it is set to binary ZERO.	

5.5 Line code

For both directions of transmission, pseudo-ternary coding is used with 100% pulse width as shown in Figure 4. Coding is performed in such a way that a binary ONE is represented by no line signal, whereas a binary ZERO is represented by a positive or negative pulse. The first binary ZERO following the frame bit-balance bit is of the same polarity as the framing bit-balance bit. Subsequent binary ZEROs must alternate in polarity.

A balance bit is a binary ZERO if the number of binary ZEROs following the previous balance bit is odd. A balance bit is a binary ONE if the number of binary ZEROs following the previous balance bit is even.

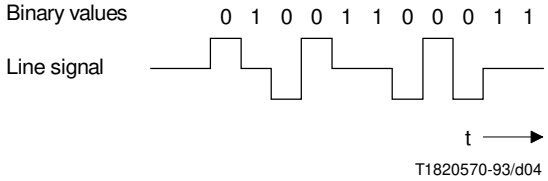


FIGURE 4/I.430

Pseudo-ternary code – Example of application

5.6 Timing considerations

The NT shall derive its timing from the network clock. A TE shall derive its timing (bit, octet, frame) from the signal received from the NT and use this derived timing to synchronize its transmitted signal.

6 Interface procedures

6.1 D-channel access procedure

The following procedure allows for a number of TEs connected in a multipoint configuration to gain access to the D-channel in an orderly fashion. The procedure always ensures that, even in cases where two or more TEs attempt to access the D-channel simultaneously, one, but only one, of the TEs will be successful in completing transmission of its information. This procedure relies upon the use of layer 2 frames delimited by flags consisting of the binary pattern "01111110" and the use of zero bit insertion to prevent flag imitation (see Recommendation I.441).

The procedure also permits TEs to operate in a point-to-point manner.

6.1.1 Interframe (layer 2) time fill

When a TE has no layer 2 frames to transmit, it shall send binary ONEs on the D-channel, i.e. the interframe time fill in the TE-to-NT direction shall be binary ONEs.

When an NT has no layer 2 frames to transmit, it shall send binary ONEs or HDLC flags, i.e. the interframe time fill in the NT-to-TE direction shall be either all binary ONEs or repetitions of the octet "01111110". When the interframe time fill is HDLC flags, the flag which defines the end of a frame may define the start of the next frame.

6.1.2 D-echo channel

The NT, on receipt of a D-channel bit from TE or TEs, shall reflect the binary value in the next available D-echo channel bit position towards the TE. (It may be necessary to force the D-echo channel bits to all binary ZEROs during certain loopbacks – see Note 4 of Table I.1 and 5/G.960.)

6.1.3 D-channel monitoring

A TE, while in the active condition, shall monitor the D-echo channel, counting the number of consecutive binary ONEs. If a binary ZERO bit is detected, the TE shall restart counting the number of consecutive binary ONE bits. The current value of the count is called C.

NOTE – C need not be incremented after the value eleven has been reached.

6.1.4 Priority mechanism

Layer 2 frames are transmitted in such a way that signalling information is given priority (priority class 1) over all other types of information (priority class 2). Furthermore, to ensure that within each priority class all competing TEs are given a fair access to the D-channel, once a TE has successfully completed the transmission of a frame, it is given a lower level of priority within the class. The TE is given back its normal level within a priority class when all TEs have had an opportunity to transmit information at the normal level within that priority class.

The priority class of a particular layer 2 frame may be a characteristic of the TE which is preset at manufacture or at installation, or it may be passed down from layer 2 as a parameter of the PH-DATA request primitive.

The priority mechanism is based on the requirement that a TE may start layer 2 frame transmission only when C (see 6.1.3) is equal to, or exceeds, the value X_1 for priority class 1 or is equal to, or exceeds, the value X_2 for priority class 2. The value of X_1 shall be eight for the normal level and nine for the lower level of priority. The value of X_2 shall be ten for the normal level and eleven for the lower level of priority.

In a priority class the value of the normal level of priority is changed into the value of the lower level of priority (i.e. higher value) when a TE has successfully transmitted a layer 2 frame of that priority class.

The value of the lower level of priority is changed back to the value of the normal level of priority when C (see 6.1.3) equals the value of the lower level of priority (i.e. higher value).

6.1.5 Collision detection

While transmitting information in the D-channel, the TE shall monitor the received D-echo channel and compare the last transmitted bit with the next available D-echo bit. If the transmitted bit is the same as the received echo, the TE shall continue its transmission. If, however, the received echo is different from the transmitted bit, the TE shall cease transmission immediately and return to the D-channel monitoring state.

6.1.6 Priority system

Annex B describes an example of how the priority system may be implemented.

6.2 Activation/deactivation

6.2.1 Definitions

6.2.1.1 TE states

6.2.1.1.1 State F1 (Inactive)

In this inactive (powered-off) state, the TE is not transmitting and cannot detect the presence of any input signals. In the case of locally powered TEs which cannot detect the appearance/disappearance of power source 1 or 2, this state is entered when local power is not present. For TEs that can detect power source 1 or power source 2, this state is entered whenever loss of power (required to support all TEI functions) is detected, or when the absence of power from power source 1 or 2, whichever power source is used for determining the connection status, is detected.

6.2.1.1.2 State F2 (Sensing)

This state is entered after the TE has been powered on but has not determined the type of signal (if any) that the TE is receiving. When in this state, a TE may go to a low-power consumption mode as specified in 5.1.8.

6.2.1.1.3 State F3 (Deactivated)

This is the deactivated state of the physical protocol. Neither the NT nor the TE is transmitting. When in this state, a TE may go to a low-power consumption mode as specified in 5.1.8.

6.2.1.1.4 State F4 (Awaiting signal)

When the TE is requested to initiate activation by means of a PH-ACTIVATE request primitive, it transmits a signal (INFO 1) and waits for a response from the NT.

6.2.1.1.5 State F5 (Identifying input)

At the first receipt of any signal from the NT, the TE ceases to transmit INFO 1 and awaits identification of signal INFO 2 or INFO 4.

6.2.1.1.6 State F6 (Synchronized)

When the TE receives an activation signal (INFO 2) from the NT, it responds with a signal (INFO 3) and waits for normal frames (INFO 4) from the NT.

6.2.1.1.7 State F7 (Activated)

This is the normal active state with the protocol activated in both directions. Both the NT and TE are transmitting normal frames. State F7 is the only state where B- and D- channel contain operational data.

6.2.1.1.8 State F8 (Lost framing)

This is the condition when the TE has lost frame synchronization and is awaiting re-synchronization by receipt of INFO 2 or INFO 4 or deactivation by receipt of INFO 0.

6.2.1.2 NT states

6.2.1.2.1 State G1 (Deactivated)

In this deactivated state, the NT is not transmitting. When in this state, an NT may go to a low-power consumption mode as specified in 5.1.8.

6.2.1.2.2 State G2 (Pending activation)

In this partially active state the NT sends INFO 2 while waiting for INFO 3. This state will be entered on request by higher layers, by means of a PH-ACTIVATE request primitive, or on the receipt of INFO 0 or lost framing while in the active state (G3). The choice to eventually deactivate is up to higher layers within the NT.

6.2.1.2.3 State G3 (Activated)

This is the normal active state where the NT and TE are active with INFO 4 and INFO 3, respectively. A deactivation may be initiated by the NT system management, by means of an MPH-DEACTIVATE request primitive, or the NT may be in the active state all the time, under non-fault conditions.

6.2.1.2.4 State G4 (Pending deactivation)

When the NT wishes to deactivate, it may wait for a timer to expire before returning to the deactivated state.

6.2.1.3 Activate primitives

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the activation procedures. For use in state diagrams, etc., abbreviations of the primitive names are also given.

PH-ACTIVATE request (PH-AR)

PH-ACTIVATE indication (PH-AI)

MPH-ACTIVATE indication (MPH-AI).

6.2.1.4 Deactivate primitives

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the deactivation procedures. For use in state diagrams, etc., abbreviations of the primitive names are also given.

PH-DEACTIVATE indication (PH-DI)

MPH-DEACTIVATE request (MPH-DR)

MPH-DEACTIVATE indication (MPH-DI).

6.2.1.5 Management primitives

The following primitives should be used between layer 1 and the management entity. For use in state diagrams, etc., abbreviations of the primitive names are also given.

MPH-ERROR indication (MPH-EI)

Message unit contains type of error or recovery from a previously reported error.

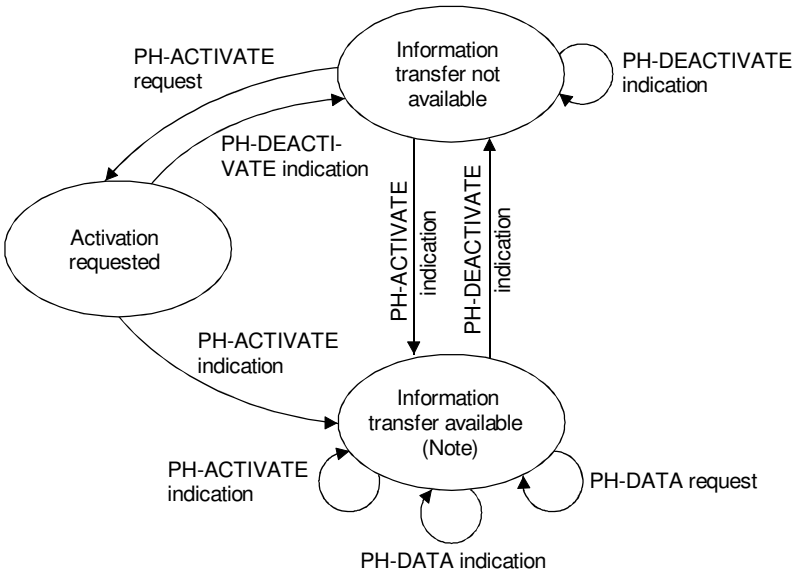
MPH-INFORMATION indication (MPH-II)

Message unit contains information regarding the physical layer conditions. Two parameters are provisionally defined : connected and disconnected.

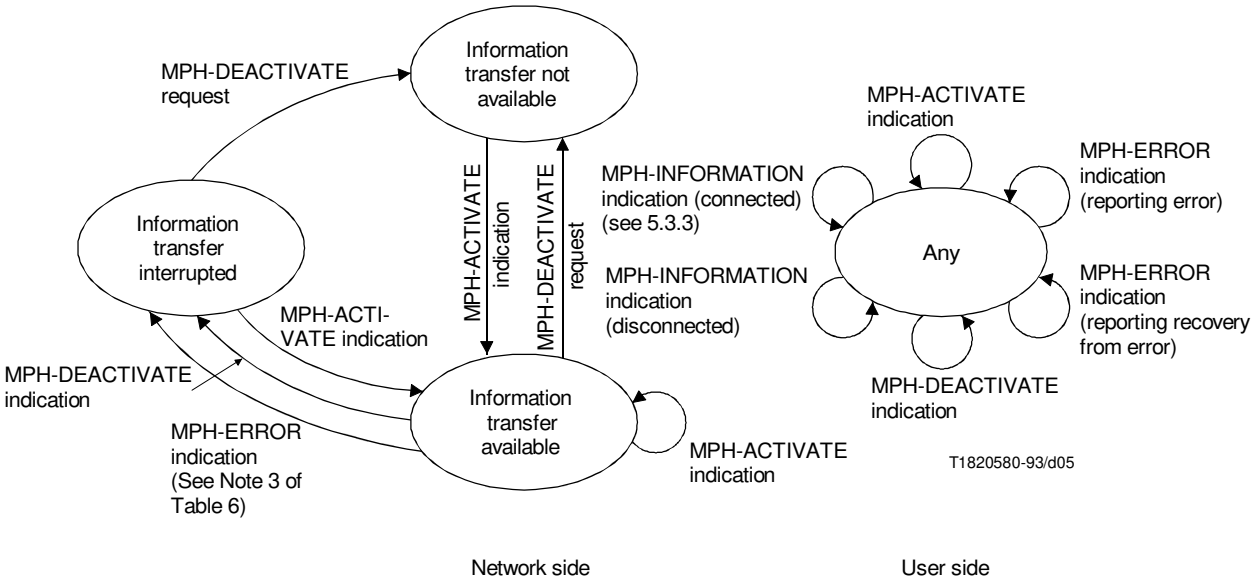
NOTE – Implementation of primitives in NTs and TEs is not for recommendation.

6.2.1.6 Valid primitive sequences

The primitives defined in 6.2.1.3, 6.2.1.4 and 6.2.1.5 specify, conceptually, the service provided by layer 1 to layer 2 and the layer 1 management entity. The constraints on the sequence in which the primitives may occur are specified in Figure 5. These diagrams do not represent the states which must exist for the layer 1 entity. However, they do illustrate the condition that the layer 2 and management entities perceive layer 1 to be in as a result of the primitives transferred between entities. Furthermore, Figure 5 does not represent an interface and is used only for modelling purposes.



a) Layer 1 – Layer 2



b) Layer 1 – Management

NOTE – Layer 2 is not aware if the information transfer capability is temporarily interrupted.

FIGURE 5/I.430

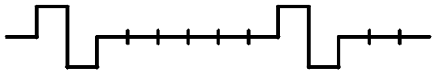
Valid primitive sequences as perceived by layer 2 and management entities

6.2.2 Signals

The definitions for specific signals across the S- or T-reference point are given in Table 4. Also included is the coding for these signals.

TABLE 4/I.430

Definition of INFO signals (Note 1)

Signals from NT to TE	Signals from TE to NT
INFO 0 (Note 4) No signal	INFO 0 (Note 4) No signal
	INFO 1 (Note 2) A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.  Nominal bit rate = 192 kbit/s
INFO 2 (Note 3) Frame with all bits of B-, D-, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.	
	INFO 3 Synchronized frames with operational data on B- and D-channels
INFO 4 (Note 3) Frames with operational data on B-, D-, and D-echo channels. Bit A set to binary ONE.	

NOTES

1 For configurations where the wiring polarity may be reversed (see § 4.3) signals may be received with the polarity of the binary ZEROs inverted. All NT and TE receivers shall be designed to tolerate wiring polarity reversals.

2 TEs which do not need the capability to initiate activation of a deactivated interface (e.g. TEs required to handle only incoming calls) need not have the capability to send INFO 1. In all other respects, these TEs shall be in accordance with 6.2. It should be noted that in the point-to-multipoint configuration more than one TE transmitting simultaneously will produce a bit pattern, as received by the NT, different from that described above, e.g. two or more overlapping (asynchronous) instances of INFO 1.

3 During the transmission of INFO 2 or INFO 4, the F_A bits and the M bits from the NT may provide the Q-bit pattern designation as described in 6.3.3.

4 For the transmission of INFO 0, the duration of a state in which the signal "consecutive binary ONEs" is transmitted is relevant rather than the definition of INFO 0 in terms of time. The duration of a state depends on events (e.g. service primitives) and may be indefinitely short.

6.2.3 Activation/deactivation procedure for TEs

6.2.3.1 General TE procedures

All TEs shall conform to the following (these statements are an aid to understanding; the complete procedures are specified in 6.2.3.2):

a) TEs, when first connected, when power is applied, or upon the loss of frame alignment (see 6.3.1.1) shall transmit INFO 0. However, a TE that is disconnected but powered is a special situation and could be transmitting INFO 1 when connected.

b) TEs shall transmit INFO 3 when frame alignment is established (see 6.3.1.2). However, the satisfactory transmission of operational data cannot be assured prior to the receipt of INFO 4.

c) TEs that are locally powered shall, when power is removed, initiate the transmission of INFO 0 before frame alignment is lost.

6.2.3.2 Specification of the procedure

The procedure for TEs which can detect power source 1 and 2 is shown in the form of a finite state matrix Table 5. An SDL representation of the procedure is outlined in Annex C. The finite state matrices for two other TE types are given in Annex C, Tables C.1 and C.2. The finite state matrix and SDL representations reflect the requirements necessary to assure proper interfacing of a TE with an NT conforming to the procedures described in Table 6. They also describe primitives at the layer 1/2 boundary and layer 1/management entity boundary.

TABLE 5/I.430

Activation/deactivation layer 1 finite state matrix for TEs
TEs powered from power source 1 or 2

Event \ State name	Inactive	Sensing	Deactivate	Awaiting signal	Identifying input	Synchronized	Activated	Lost framing
State number	F1	F2	F3	F4	F5	F6	F7	F8
INFO Sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
Power on and detection of Power S (Notes 1 and 2)	F2	–	–	–	–	–	–	–
Disappearance of Power S (Notes 1 and 2)	–	F1	MPH-II(d), F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1
PH-ACTIVATE-REQUEST	/	|	ST T3; F4	|	|	–	|	–
Expiry T3 (Note 7)	/	/	–	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, (Note 8)	/	MPH-DI, PH-DI, F3
RECEIVE INFO 0 (Notes 5 and 6)	/	MPH-II(c), F3	–	–	–	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, MPH-EI2, F3
Receive any signal (Note 3)	/	–	–	F5	–	/	/	–
Receive INFO 2	/	MPH-II(c), F6	F6	F6 (Note 4)	F6	–	MPH-EI1, F6	MPH-EI2, F6
Receive INFO 4	/	MPH-II(c), PH-AI, MPH-AI, F7	PH-AI, MPH-AI, S/R T3 F7	PH-AI, MPH-AI, S/R T3 F7 (Note 4)	PH-AI, MPH-AI, S/R T3 F7	PH-AI, MPH-AI, MPH-EI2, S/R T3 F7	–	PH-AI, MPH-AI, MPH-EI2, S/R T3 F7
Lost framing	/	/	/	/	/	MPH-EI1 F8	MPH-EI1 F8	–

–	No change, no action
|	Impossible by the definition of the layer 1 service
/	Impossible situation
a, b, Fn	Issue primitives “a” and “b” and then go to state “Fn”
PH-AI	Primitive PH-ACTIVATE indication
PH-DI	Primitive PH-DEACTIVATE indication
MPH-AI	Primitive MPH-ACTIVATE indication
MPH-DI	Primitive MPH-DEACTIVATE indication
MPH-EI1	Primitive MPH-ERROR indication reporting error
MPH-EI2	Primitive MPH-ERROR indication reporting recovery from error
MPH-II(c)	Primitive MPH-INFORMATION indication (connected)
MPH-II(d)	Primitive MPH-INFORMATION indication (disconnected)
ST T3	Start Timer T3
S/R T3	Stop/Reset T3
power S	Power source 1 or power source 2.

TABLE 5/I.430 *(end)*

Activation/deactivation layer 1 finite state matrix for TEs
TEs powered from power source 1 or 2

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time.

NOTES

1 The term "power" could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI value in memory and maintain the capability of receiving and transmitting layer 2 frames associated with the TEI procedures.

2 The procedures described in this Table require the provision of power source 1 or power source 2 to enable their complete operation. A TE which determines that it is connected to an NT not providing power source 1 or 2 should default to the procedures described in Table C.1.

3 This event reflects the case where a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.

4 If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs must go to state F5. To assure that a TE will go to state F5 when receiving a signal to which it cannot synchronize, operation of TEs should be verified where the received signal is any bit pattern (containing at least 3 binary ZEROs in each frame interval) to which TEs conforming to 6.3.1.2 are not able to synchronize.

5 INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the TE shall perform the actions specified in this Table.

For conformance test purposes, when in the states F6 and F7 with a sinusoidal signal having a voltage of 100 mV peak-to-peak superimposed on the received signal, the TE shall react to INFO 0 by transmitting INFO 0 within a period of time 250 µs to 25 ms.

It is recognized that the action in states F2 and F8 is the passing of a primitive and that this cannot be observed or verified at the interface.

A provision for the immediate reaction to INFO 0 following the receipt of 48 contiguous binary ONEs may cause the release of ongoing communications in response to spurious interface signal interruptions. A persistence check time should be considered to minimize such a possibility, but the total reaction time shall not exceed 25 ms.

6 To avoid disruption of an on-going communication caused by spurious effects, a timer may be started when leaving the state F7 or F8 upon reception of INFO 0. The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter state F7 before expiry of this timer. The value of this timer may be in the range of 500 ms to 1000 ms.

7 Timer 3 (T3) is a supervisory timer which has to take into account the overall time to activate. This time includes the time it takes to activate both the ET-NT and the NT-TE portion of the customer access.

8 Terminals may momentarily enter state F3 at this point and return to state F6 if INFO 2 is still being received (the term "momentary" means up to a maximum of 5 frames).

6.2.4 Activation/deactivation for NTs

6.2.4.1 Activating/deactivating NTs

The procedure is shown in the form of a finite state matrix in Table 6. An SDL representation of the procedure is outlined in Annex C. The finite state matrix and SDL representations reflect the requirements necessary to assure proper interfacing of an activating/deactivating NT with a TE conforming to the procedures described in Table 5. They also describe primitives at the layer 1/2 boundary and layer 1/mangement entity boundary.

6.2.4.2 Non-activating/non-deactivating NTs

The behaviour of such NTs is the same as that of an activating/deactivating NT never receiving MPH-DEACTIVATE request from the management entity. States G1 (Deactivated), G4 (Pending deactivation) and timers 1 and 2 may not exist in such NTs.

6.2.5 Timer values

The finite state matrix tables show timers on both the TE and the NT. The following values are defined for timers :

- TE: Timer 3, not to be specified (the value depends on the subscriber loop transmission technique. The worst case value is 30 s).
- NT: Timer 1, not to be specified. Timer 2, 25 to 100 ms.

TABLE 6/I.430

Activation/deactivation layer 1 finite state matrix for NTs

	State name	Deactivated	Pending Activation	Activated	Pending deactivation
	State number	G1	G2	G3	G4
Event	INFO sent	INFO 0	INFO 2	INFO 4	INFO 0
PH-ACTIVATE request		Start timer T1 G2	|	|	Start timer T1 G2
MPH-DEACTIVATE request		|	Start timer T2, PH-DI; G4 (Note 2)	Start timer T2, PH-DI; G4 (Note 2)	|
Expiry T1 (Note 1)		–	Start timer T2, PH-DI; G4 (Note 2)	/	–
Expiry T2		–	–	–	G1
Receiving INFO 0 (Note 5)		–	–	MPH-DI, MPH-EI; G2 (Note 3)	G1
Receiving INFO 1		Start timer T1 G2	–	/	–
Receiving INFO 3		/	Stop timer T1 PH-AI, MPH-AI; G3 (Note 4)	–	–
Lost Framing		/	/	MPH-DI, MPH-EI; G2 (Note 3)	–

–	No state change
/	Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons
|	Impossible by the definition of the physical layer service
a ,b; Gn	Issue primitives “a” and “b” then go to state “Gn”
PH-AI	Primitive PH-ACTIVATE indication
PH-DI	Primitive PH-DEACTIVATE indication
MPH-AI	Primitive MPH-ACTIVATE indication
MPH-DI	Primitive MPH-DEACTIVATE indication
MPH-EI	Primitive MPH-ERROR indication

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time.

NOTES

1 Timer 1 (T1) is a supervisory timer which has to take into account the overall time to activate. This time includes the time it takes to activate both the ET-NT and the NT-TE portion of the customer access. ET is the exchange termination.

2 Timer 2 (T2) prevents unintentional reactivation. Its value is 25 ms ≤ value ≤ 100 ms. This implies that a TE has to recognize INFO 0 and to react to it within 25 ms. If the NT is able to unambiguously recognize INFO 1, then the value of timer 2 may be 0, and an MPH-DEACTIVATE request would cause a direct transition from state G2 or G3 to G1. It should be noted that the unambiguous detection of INFO 1 may not be possible in passive bus configurations, considering all possible implementations.

3 These notifications (MPH-DI, MPH-EI) need not be transferred to a management entity at the NT.

4 As an implementation option, to avoid premature transmission of information (i.e. INFO 4), layer 1 may not initiate the transmission of INFO 4 or send the primitives PH-ACTIVATE indication and MPH-ACTIVATE indication (to layer 2 and management, respectively) until a period of 100 ms has elapsed since the receipt of INFO 3. Such a delay time should be implemented in the ET, if required.

5 INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the NT shall perform the actions specified in this Table.

For conformance test purposes, when in the state G3 with a sinusoidal signal having a voltage of 100 mV peak-to-peak superimposed on the received signal, the NT shall react to INFO 0 by transmitting INFO 2 after a period of time equal or greater than 250 µs.

It is recognized that the action in state G4 cannot be observed or verified at the interface.

6.2.6 Activation times

6.2.6.1 TE activation times

A TE in the deactivated state (F3) shall, upon the receipt of INFO 2 or INFO 4, establish frame synchronization and initiate the transmission of INFO 3 within 100 ms. A TE shall recognize the receipt of INFO 4 within two frames (in the absence of errors).

A TE in the "awaiting signal" state (F4) shall, upon the receipt of INFO 2 or INFO 4, cease the transmission of INFO 1 and initiate the transmission of INFO 0 within 5 ms and then respond to INFO 2 or INFO 4, within 100 ms, as above. (Note that in Table 5, the transition from F4 to F5 is indicated as the result of the receipt of "any signal" which is in recognition of the fact that a TE may not know that the signal being received is INFO 2 or INFO 4 until after it has recognized the presence of a signal.)

6.2.6.2 NT activation times

An NT in the deactivated state (G1) shall, upon the receipt of INFO 1, initiate the transmission of INFO 2 (synchronized to the network) within 1 s under normal conditions. Delays, "Da", as long as 30 s are acceptable under abnormal (non-fault) conditions, e.g. as a result of a need for retrain for an associated loop transmission system.

An NT in the "pending activation" state (G2) shall, upon the receipt of INFO 3, initiate the transmission of INFO 4 within 500 ms under normal conditions. Delays, "Db", as long as 15 s are acceptable under abnormal (non-fault) conditions provided that the sum of the delays "Da" and "Db" is not greater than 30 s.

6.2.7 Deactivation times

A TE shall respond to the receipt of INFO 0 by initiating the transmission of INFO 0 within 25 ms.

An NT shall respond to the receipt of INFO 0 or the loss of frame synchronization by initiating the transmission of INFO 2 within 25 ms; however, the layer 1 entity does not deactivate in response to INFO 0 from a TE.

6.3 Frame alignment procedures

The first bit of each frame is the framing bit, F; it is a binary ZERO.

The frame alignment procedure makes use of the fact that the framing bit is represented by a pulse having the same polarity as the preceding pulse (line code violation). This allows rapid reframing.

According to the coding rule, both the framing bit and the first binary ZERO bit following the framing bit-balance bit (in position 2 in the same frame) produce a line code violation. To guarantee secure framing, the auxiliary framing bit pair F_A and N in the direction NT to TE or the auxiliary framing bit F_A with the associated balancing bit L in the direction TE to NT are introduced. This ensures that there is a line code violation at 14 bits or less from the framing bit F, due to F_A or N being a binary ZERO bit (NT to TE) or to F_A being a binary ZERO bit (TE to NT) if the F_A-bit position is not used as a Q bit. The framing procedures do not depend on the polarity of the framing bit F, and thus are not sensitive to wiring polarity.

The coding rule for the auxiliary framing bit pair F_A and N, in the direction NT to TE, is such that N is the binary opposite of F_A ($N = \overline{F_A}$). The F_A and L bits in the direction TE to NT are always coded such that the binary values of F_A and L are equal.

6.3.1 Frame alignment procedure in the direction NT to TE

Frame alignment, on initial activation of the TE, shall comply with the procedures defined in 6.2.

6.3.1.1 Loss of frame alignment

Loss of frame alignment may be assumed when a time period equivalent to two 48-bit frames has elapsed without having detected valid pairs of the line code violations obeying the ≤14-bit criterion as described above. The TE shall cease transmission immediately.

6.3.1.2 Frame alignment

Frame alignment may be assumed to occur when three consecutive pairs of line code violations obeying the ≤ 14-bit criterion have been detected.

6.3.2 Frame alignment in the direction TE to NT

The criterion of a line code violation at 13 bits or less from the framing bit (F) shall apply except if the Q-channel (see 6.3.3) is provided, in which case the 13-bit criterion applies in four out of five frames.

6.3.2.1 Loss of frame alignment

The NT may assume loss of frame alignment if a time period equivalent to at least two 48-bit frames has elapsed since detecting consecutive violations according to the 13-bit criterion, if all F_A bits have been set to binary ZERO. Otherwise, a time period equivalent to at least three 48-bit frames shall be allowed before assuming loss of frame alignment. On detection of loss of frame alignment the NT shall continue transmitting towards the TE.

6.3.2.2 Frame alignment

The NT may assume that frame alignment has been regained when three consecutive pairs of the line code violations obeying the 13-bit criterion have been detected

6.3.3 Multiframing

Multiframing provides a layer 1 signalling capability between the TEs and the NT in both directions through the use of extra channels referred to as the S-channel for the NT-to-TE direction and the Q-channel for the TE-to-NT direction. This layer 1 signalling capability exists only between the TE and NT, i.e. there is no requirement in the NT for the transfer of signals between the TE-NT channels and the layer 1 signalling channel between the NT and the network.

The use of the Q- and S-channels shall be the same in point-to-point as in point-to-multipoint configurations. There is no inherent collision detection mechanism provided for the Q-channel, nor is there any addressing mechanism for the S-channel. Procedures necessary to prevent or deal with collision and to indicate the desired TEs that are required for any application are not a part of this Recommendation.

The uses of the Q-channels and S – channels are optional. NTs that do not support these channels are not required to encode the F_A and M bits as required for the defined multiframing. TEs that do not use the Q-bit channel must set each Q bit to a binary ONE in each frame in which a binary ONE is received in the F_A-bit position of the NT-to-TE frame (i.e. echoing of the received F_A bits).

6.3.3.1 General mechanism

a) *Q-bit identification* – The Q bits (TE-to-NT) are defined to be the bits in the F_A bit position of every fifth frame. The Q-bit positions in the TE-to-NT direction are identified by binary inversions of the F_A/N-bit pair (F_A = binary ONE, N = binary ZERO) in the NT-to-TE direction. The provision of this capability in NTs is optional. The provision for identification of the Q-bit positions in the NT-to-TE direction permits all TEs to synchronize transmission in Q-bit positions thereby avoiding interference of F_A bits from one TE with the Q bits of a second TE in passive bus configurations.

b) *Multiframe identification* – A multiframe, which provides for structuring the Q bits into 4-bit characters (Q1 - Q4), is established by setting the M bit, in bit position 26 (see 5.4.2.2) of the NT-to-TE frame, to binary ONE in every twentieth frame. This structure provides for 4-bit characters in a single channel, TE-to-NT. The provision of this capability in NTs is optional. Detection and use of the M bit by the TE is optional if the Q-channel is not intended to be used.

6.3.3.2 Q-Bit position identification algorithm

The Q-bit position identification algorithm is illustrated in Table 7. The TE synchronizes to the received F_A bit inversions and transmits Q bits in every fifth frame, i.e. in frames in which F_A bits (NT-to-TE direction) should be equal to binary ONE. The algorithm used by a TE to determine multiframe synchronization or loss of multiframe

synchronization is not described in this Recommendation. However, a TE should echo the received Q-bit position identifier (F_A bit) into the TE-to-NT Q-bit position when multiframe synchronization is not established.

No special Q-bit identification derived from the received signal is required in the NT because the maximum round trip delay of NT-to-TE-to-NT is a small fraction of a frame, and, therefore, Q-bit identification is inherent in the NT.

TABLE 7/I.430

Q-bit position identification and multi-frame structure

Frame number	NT-to-TE F_A bit position	NT-to-TE M Bit	TE-to-NT F_A bit position (Notes 1 and 2)
1	ONE	ONE	Q1
2	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO
6	ONE	ZERO	Q2
7	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO
11	ONE	ZERO	Q3
12	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO
16	ONE	ZERO	Q4
17	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO
1	ONE	ONE	Q1
2	ZERO	ZERO	ZERO
etc.			

NOTES

1 If the Q-bits are not used by a TE, the Q-bits shall be set to binary ONE.

2 Where multiframe identification is not provided with a binary ONE in an appropriate M bit, but where Q-bit positions are identified, Q bits 1 through 4 are not distinguished.

6.3.3.3 TE Multiframe identification

The first frame of the multiframe is identified by the M bit equal to a binary ONE. TEs that are not intended to use nor to provide for the use of the Q-channel, are not required to identify the multiframe. TEs that are intended to use, or to provide for the use of, the Q-channel shall use the M bit equal to a binary ONE to identify the start of the multiframe.

The algorithm used by a TE to determine when synchronization or loss of synchronization of the multiframe is achieved is not described in this Recommendation; however, it should be noted that the transmission of multiframing from an NT is not mandatory.

6.3.4 S-channel structuring algorithm

The algorithm for structuring the S bits [NT-to-TE frame bit position 37 (see 5.4.2.2)] into an S-channel uses the same combination of the F_A bit inversions and the M bit that is used to structure the Q-channel as described in 6.3.3. The S-channel structure, shown in Table 8, provides for five subchannels, SC1 through SC5. Each subchannel SC*n* is comprised of the bits SC*n*1 through SC*n*4, which provide for the transfer of one 4-bit character per multiframe (5 ms).

Use of the five channels is specified in 7.

TABLE 8/I.430

S-channel structure

Frame number	NT-to-TE F_A-bit position	NT-to-TE M bit	NT-to-TE S bit
1	ONE	ONE	SC11
2	ZERO	ZERO	SC21
3	ZERO	ZERO	SC31
4	ZERO	ZERO	SC41
5	ZERO	ZERO	SC51
6	ONE	ZERO	SC12
7	ZERO	ZERO	SC22
8	ZERO	ZERO	SC32
9	ZERO	ZERO	SC42
10	ZERO	ZERO	SC52
11	ONE	ZERO	SC13
12	ZERO	ZERO	SC23
13	ZERO	ZERO	SC33
14	ZERO	ZERO	SC43
15	ZERO	ZERO	SC53
16	ONE	ZERO	SC14
17	ZERO	ZERO	SC24
18	ZERO	ZERO	SC34
19	ZERO	ZERO	SC44
20	ZERO	ZERO	SC54
1	ONE	ONE	SC11
2	ZERO	ZERO	SC21
etc.			

NOTE – S-subchannels not used by the NT1 shall be set to all binary ZEROs.

6.4 Idle channel code on the B-channels

A TE shall send binary ONEs in any B-channel that is not assigned to it.

7 Layer 1 maintenance

7.1 Provision for operational and maintenace functions between terminal and NT1

Equipment implementing the optional functionalities in the S- and Q-channels shall be in accordance with this subclause.

7.1.1 Introduction

As indicated in 6.3.3, maintenance function signalling channels may be provided in both the NT-to-TE and TE-to-NT directions. This subclause describes the optional use of those channels. The functions to be signalled on these channels and the associated protocol are specified in the following subclauses. The provision of the functions in TEs and NTs is optional, but, where a function is provided, the signals shall be as specified.

In the following discussion, the generic term "TE" refers to either a TE connected to an NT1, a TE connected to an NT2, or an NT2 connected to an NT1. Also the generic term "NT" can be either an NT1 or an NT2 to which a TE (generic meaning) is connected.

This subclause discusses the optional use of the Q-channel and the SC1 subchannel. Subchannels SC2 through SC5 are reserved for future specification and should be coded with all binary ZEROs.

7.1.2 Test loopbacks

The test loopbacks defined for the basic user-network interface are specified in Appendix I.

Loopbacks for which layer 1 control is specified are indicated in Figure I.1 as loopback C in the NT1 and loopback B1 or B2 in the NT2. The characteristics of the two loopbacks are specified in Table I.2.

7.1.3 Codes, message durations, and detection algorithms for a Q-channel and SC1-subchannel

The codes for all the Q-channels and SC1-subchannels are defined in Table 9. Each code is a four-bit character transmitted in a single multiframe.

One of the several codes that are reserved for future standardization could be defined in the future as an escape code to extend the number of messages if that ever becomes necessary.

Except where stated otherwise, the code for a message shall be repeated in at least six consecutive Q or SC1 characters or as many times as necessary to obtain the desired response (e.g. loopback).

Except where stated otherwise, a message shall be considered received only when the proper code is received in three consecutive Q or SC1 characters.

7.1.4 Code priorities for Q-channel and SC1-subchannel

The following rules apply for interruption of the sending of one code by another:

1) Loss of power (LP) always takes precedence.

2) Self Test (ST) request, indication, pass and fail take precedence over all other codes except LP.

3) Report of error (DTSE) is instantly sent (once) and replaces one occurrence of whatever else was being sent (except LP and ST).

   NOTE – DTSE messages should not be sent when signal has been lost at the network side of the NT1.

(4) Loopback requests (LB) and confirmations can interrupt only three codes: idle, disruptive operation indication, and loss of received signal.

(5) Loss of received signal (LRS) replaces idle or disruptive operation indication whenever the loss is detected by the NT.

(6) Disruptive NT operation indication (DOI) cannot interupt any other codes except Idle.

(7) NORMAL is the idle code when no other codes are present.

7.1.5 TE-to-NT direction messages (Q bits)

The codes for the Q-channel messages are defined in Table 9.

TABLE 9/I.430

Definition of SC1 and Q-channel

Message (Notes 1 and 2)	Code used in direction							
	NT-to-TE				TE-to-NT			
	SC11	SC12	SC13	SC14	Q1	Q2	Q3	Q4
Idle (NORMAL)	0	0	0	0	1	1	1	1
Loss of power indication	1	1	1	1	0	0	0	0
STP pass	0	0	1	0	–	–	–	–
STF fail	0	0	0	1	–	–	–	–
ST request (Note 3)	–	–	–	–	0	0	0	1
STI indication	0	1	1	1	–	–	–	–
DTSE-IN&OUT	1	1	0	0	–	–	–	–
DTSE-IN	1	0	0	0	–	–	–	–
DTSE-OUT	0	1	0	0	—	–	–	–
LB1 request	–	–	–	–	0	1	1	1
LB1I indication	1	1	0	1	–	–	–	–
LB2 request	–	–	–	–	1	0	1	1
LB2I indication	1	0	1	1	–	–	–	–
LB1/2 request (Note 4)	–	–	–	–	0	0	1	1
LB1/2I indication	1	0	0	1	–	–	–	–
Loss of received Signal indication	1	0	1	0	–	–	–	–
Disruptive operation indication	0	0	1	1	–	–	–	–

Message (Notes 5 and 2)	Code used in direction							
	NT-to-TE				TE-to-NT			
	SC11	SC12	SC13	SC14	Q1	Q2	Q3	Q4
V-DTE slave mode	–	–	–	–	1	1	0	1
V-DCE slave mode	–	–	–	–	1	1	0	0
V-DCE master mode	0	1	1	0	–	–	–	–

These three reserved codes should only be used by devices configured to be V-DTEs or V-DCEs.

NOTES

1 Codes not specified in the above table and not listed below as reserved are for future standardisation.

2 Except for the idle code, the codes are in the order of priority.

3 The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a passive bus.

4 The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a bus.

5 The following message codes have been reserved for Recommendation V.230.

7.1.5.1 Idle channel (NORMAL)

The NORMAL message shall be transmitted during normal conditions, i.e. at all times when no other message is being transmitted. The continuous transmission of the NORMAL message assures that spurious unintended loopbacks or conditions are cleared quickly.

This will be the usual message to request the release of a loopback.

7.1.5.2 Loss-of-power indication (LP)

This message is an indication to the NT that the TE has lost power. This LP message should be transmitted in at least one but no more than 3 multiframes just prior to the initiation of the transmission of INFO 0 before frame alignment is lost [see 6.2.3.1 c)]. The transmission of this indication requires the TE to have sufficient energy storage to maintain proper transmission for at least two full multiframes (10 ms).

7.1.5.3 Request self test (ST)

The TE can request that the NT perform a self test. The scope of the self test is not defined. The self test report returning from the NT1 shall be pass (STP) or fail (STF). The use of the ST message by a TE connected to an NT2 is for further study.

7.1.5.4 Request a loopback (LB1, LB2, LB1/2)

The two loopback request messages are designated LB1 (request loopback of channel B1) and LB2 (request loopback of channel B2). For example, a TE that is currently assigned to transmit over the B1 channel may send LB1 across the interface (at reference points S or T) to request a loopback in the NT of channel B1. These LB1 and LB2 messages are coded in such a way that the two different loopbacks can be requested at the same time by two different TEs on a bus. The resulting message that is received by the NT is defined as LB1/2. One TE will use the B1 channel looped back while the other TE uses the B2 channel looped back. LB1/2 may also originate from a single TE.

Each loopback shall remain established as long as the NT continues to receive the appropriate message (LB1, LB2, or LB1/2) from the TEs. Any other message that is properly received from the TEs will cause the release of the loopback(s). The NORMAL message is the usual way of requesting the release of a loopback.

7.1.6 NT-to-TE direction messages (SC1 bits).

The codes for the SC1-subchannel messages are defined in Table 9. Use of the SC1 subchannel remains optional.

7.1.6.1 Idle channel (NORMAL)

The NORMAL message shall be transmitted during normal conditions, i.e. at all times when no other message is being transmitted. The continuous transmission of the NORMAL message assures that spurious unintended conditions are cleared quickly.

7.1.6.2 Loss-of-power indication (LP)

This is an indication to the TEs that the NT has lost power. This LP message should be transmitted in at least one multiframe. The transmission of this indication requires the NT to have sufficient energy storage to maintain proper transmission for at least two multiframes (about 10 ms).

7.1.6.3 Detected access transmission system error (DTSE-OUT, DTSE-IN)

This message is an indication to the TEs from the NT1 that a basic access system performance monitoring capability has indicated an error in a block of bits.

NOTE – DTSE messages shall not be sent when signal has been lost at the network side of the NT1.

It is assumed that the performance monitoring capability will independently indicate errors for each of the two directions of transmission. Therefore, two indications are provided: error-out and error-in for errors that are detected in the transmitted (from the NT1) direction and errors in the received (to the NT1) direction, respectively.

The DTSE messages should be transmitted once for each time that a performance monitored block is detected to contain an error. Therefore, it is recognized that, when the interface error rate is high, this information can be corrupted.

In cases where performance monitoring capability is intentionally corrupted (e.g. for testing the error detection mechanism), the transmission of any corresponding DTSEs toward the TEs shall be suppressed. Table 10 defines the conditions in which the transmission of each DTSE message is suppressed, and also identifies the incoming network side indicator expected to report a performance monitoring (PM) error (crc is cyclic redundancy check, febe is far-end block error).

TABLE 10/I.430

Suppression of DTSE messages

SC1	When suppressed	PM indicator
DTSE-IN	Notified of corruption	crc
DTSE-OUT	Corruption requested	febe
DTSE-IN/OUT	Both notified and requested	crc and febe

7.1.6.4 Self test indication

This message indicates to the TEs that the NT is in a self test mode. The message should continue to be transmitted until the NT completes the self test.

NOTE – It is assumed that transmission on the D-channel as well as on the B-channels may be interrupted during the self test.

7.1.6.5 Self test report (STP, STF)

This message is a report to the TEs of an NT self test that was requested by a TE. The report shall indicate pass (STP) or fail (STF).

7.1.7 B-Channel loopback indications (LB1I, LB2I, LB1/2I)

This message indicates to the TEs that the NT is looping back B-channel 1 (LB1I) or B-channel 2 (LB2I), or both (LB1/2I), toward the TEs. This message continues to be transmitted as long as the loopback remains active.

7.1.8 Loss-of-received-signal indication (LRS)

This message is an indication to the TEs that the NT cannot properly identify the signal that is being received across the interface at the network side of the NT. A loss of frame synchronization is considered one condition when the LRS message should be transmitted toward the TE.

Note – In some applications the loss of received signal may also result in the "A" bit being set to binary ZERO.

This message should be sent continuously in all multiframes until the condition is cleared. This message shall obey the criteria for reception and transmission as stated in 7.1.3.

7.1.9 Disruptive NT operation indication (DOI)

This message is an indication to the TEs that the NT is operating under a condition that may disrupt the normal flow of D-channel messages. Several examples of D-channel disruption are as follows:

1) Looping back the full 2B + D user data stream toward the network.

2) An indication from the network that it has lost transparency and cannot operate on D-channel messages.

3) An operator initiated NT test that causes the NT to disrupt the D-channel message flows in either direction.

4) Any network generated alarm that indicates disruption of D-channel messages.

5) Any further user or network side action that would disrupt the D-channel operation or would remove the D-channel from service.

This message continues to be transmitted as long as the potentially disruptive operation remains active.

8 Electrical characteristics

8.1 Bit rate

8.1.1 Nominal rate

The nominal bit rate is 192 kbit/s.

8.1.2 Tolerance

The tolerance (free running mode) is ±100 ppm.

8.2 Jitter and bit-phase relationship between TE input and output

8.2.1 Test configurations

The jitter and phase deviation measurements are carried out with four different waveforms at the TE input, in accordance with the following configurations:

i) point-to-point configuration with 6 dB attenuation measured between the two terminating resistors at 96 kHz (high capacitance cable);

ii) short passive bus with 8 TEs (including the TE under test) clustered at the far end from the signal source (high capacitance cable);

iii) short passive bus with the TE under test adjacent to the signal source and the other seven TEs clustered at the far end from the signal source. Configuration a) high capacitance cable; configuration b) low capacitance cable;

iv) ideal test signal condition, with one source connected directly to the receiver of the TE under test (i.e. without artificial line).

Examples of waveforms that correspond to the configurations i), ii), iii a) and iii b) are given in Figures 6 to Figure 9. Test configurations which can generate these signals are given in Annex D.

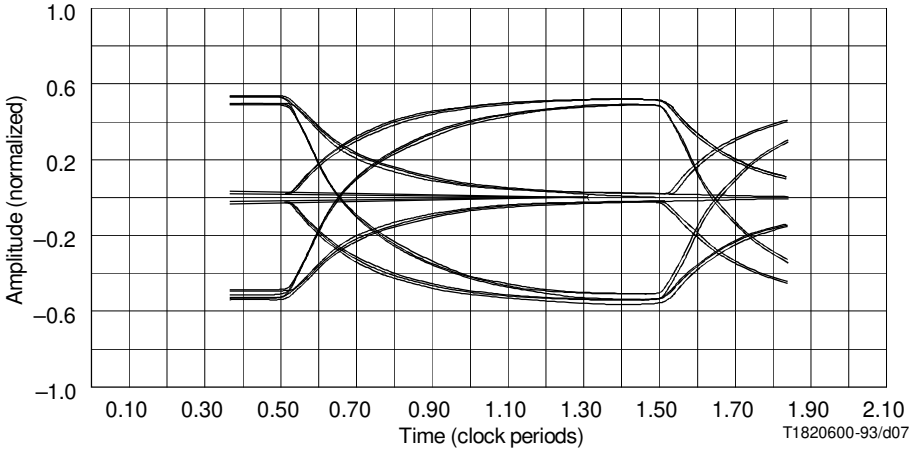


FIGURE 6/I.430

Waveform for test configuration i) – Point-to-point (6 dB)
(C = 120 nF/km)

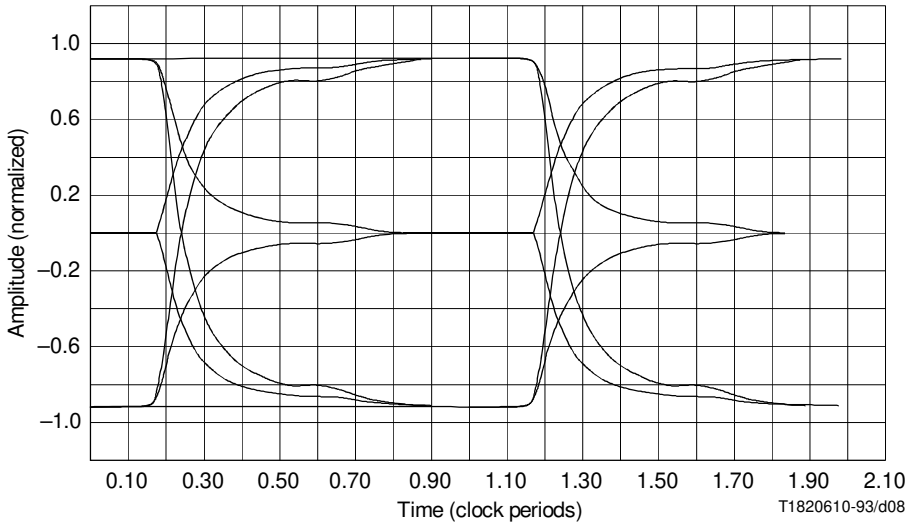


FIGURE 7/I.430

Waveform for test configuration ii) – Short passive bus with eight clustered TEs at the far end (C = 120 nF/km)

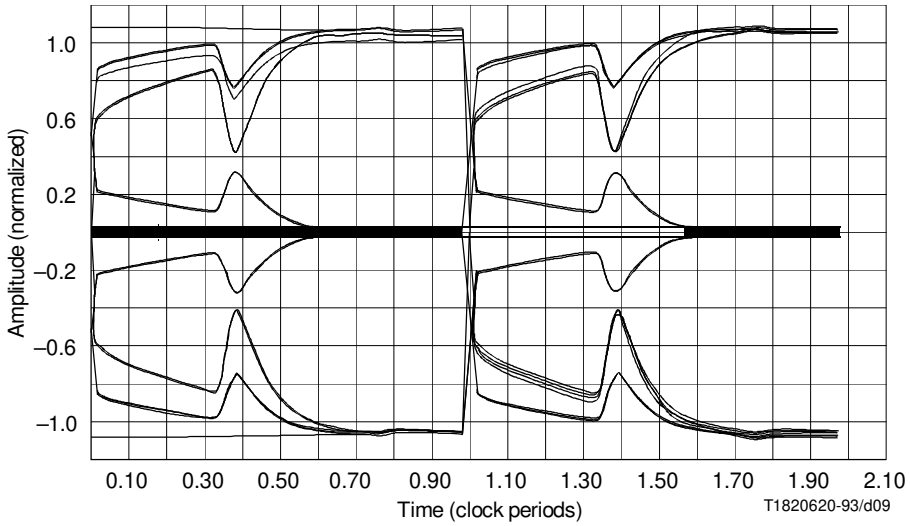


FIGURE 8/I.430

Waveform for test configuration iii) a) – Short passive bus with one TE near to NT, and seven TEs at the far end (C = 120 nF/km)

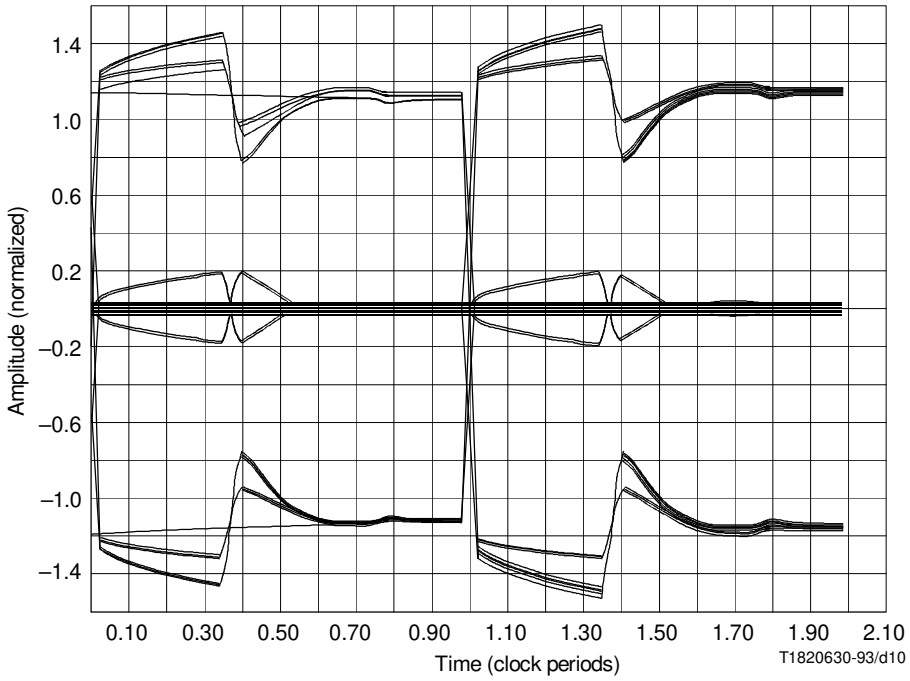


FIGURE 9/I.430

Waveform for test configuration iii) b) – Short passive bus with one TE near to NT, and seven TEs at the far end (C = 30 nF/km)

8.2.2 Timing extraction jitter

Timing extraction jitter, as observed at the TE output, shall be within −7% to +7% of a bit period, when the jitter is measured using a high pass filter with a cut-off frequency (3 dB point) of 30 Hz and an asymptotic roll off 20 dB per decade under the test conditions described in 8.2.1. The limitation applies with an output data sequence having binary ONEs in both B-channels and with input data sequences described in a) to c) below. The limitation applies to the phase of all zero-volt crossings of all adjacent binary ZEROs in the output data sequence.

a) a sequence consisting of continuous frames with all binary ONEs in D-channel, D-echo channel and both B-channels;

b) a sequence, repeated continuously for at least 10 seconds, consisting of

   – 40 frames with continuous octets of "10101010" (the first bit to be transmitted is binary ONE) in both B-channels and continuous binary ONEs in D-channel and D-echo channel, followed by

   – 40 frames with continuous binary ZEROs in D-channel , D-echo channel and both B-channels;

c) a sequence consisting of a pseudo random pattern with a length of $2^{19} - 1$ in D-channel, D-echo channel, and both B-channels. [This pattern may be generated with a shift register with 19 stages with the outputs of the first, the second, the fifth and the nineteenth stages added together (modulo 2) and fed back to the input.]

8.2.3 Total phase deviation input to output

The total phase deviation (including effects of timing extraction jitter in the TE), between the transitions of signal elements at the output of the TE and the transitions of signal elements associated with the signal applied to the TE input, should not exceed the range of −7% to +15% of a bit period. This limitation applies to the output signal transitions of each frame with the phase reference defined as the average phase of the crossing of zero, which occurs between the framing pulse and its associated balance pulse at the start of the frame and corresponding crossings at the start of the three preceding frames of the input signal.

For the purpose of demonstrating compliance of an equipment, it is sufficient to use (as the input signal phase reference) only the crossing of zero volts between the framing pulse and its associated balance pulse of the individual frame. This latter method, requiring a simpler test set, may create additional jitter at frequencies higher than about 1 kHz and is therefore more restrictive. The limitation applies to the phase of the zero-volt crossings of all adjacent binary ZEROs in the output data sequence, which shall be as defined in 8.2.2. The limitation applies under all test conditions described in 8.2.1, with the additional input signal conditions specified in a) to d) below, and with the superimposed jitter as specified in Figure 10 over the range of frequencies from 5 Hz to 2 kHz. The limitation applies for input bit rates of 192 kbit/s ± 100 ppm.

a) A sequence consisting of continuous frames with all binary ONEs in the D-channel , D-echo channel and both B-channels.

b) A sequence consisting of continuous frames with the octet "10101010" (the first bit to be transmitted is binary ONE) in both B-channels and binary ONEs in D-channel and D-echo channel;

c) A sequence of continuous frames with binary ZEROs in D-channel, D-echo channel and both B-channels.

d) A sequence of continuous frames with a pseudo random pattern, as described in 8.2.2 c), in D-channel, D-echo channel and both B-channels.

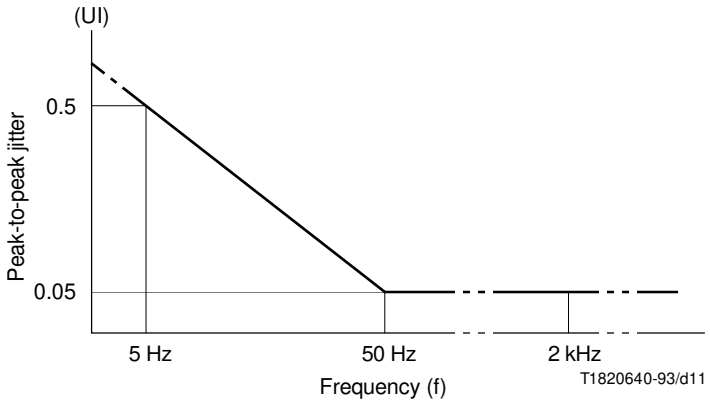


FIGURE 10/I.430

Lower limit of maximum tolerable jitter at TE input (log-log scale)

8.3 NT jitter characteristics

The maximum jitter (peak-to-peak) in the output sequence of an NT shall be 5% of a bit period when measured using a high pass filter having a cut-off frequency (3 dB point) of 50 Hz and an asymptotic roll off of 20 dB per decade. The limitation applies for all data sequences, but for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure jitter with an output data sequence consisting of binary ONEs in D- and B-channels and with an additional sequence as described in 8.2.2 c) in D- and B-channels. The limitation applies to the phase of all zero-volt crossings of all adjacent binary ZEROs in the output data sequence.

8.4 Termination of the line

The interchange circuit pair termination (resistive) should be 100 ohms ± 5% (see Figure 2).

8.5 Transmitter output characteristics

8.5.1 Transmitter output impedance

The following requirements apply at interface point I_A (see Figure 2) for TEs and at interface point I_B for NTs (see 4.5 and 8.9 regarding capacitance of the cord).

8.5.1.1 NT transmitter output impedance

a) At all times except when transmitting a binary ZERO, the output impedance, in the frequency range of 2 kHz to 1 MHz, shall exceed the impedance indicated by the template in Figure 11. The requirement is applicable with an applied sinusoidal voltage of 100 mV (rms value).

NOTE – In some applications, the terminating resistor can be combined with the NT (see point B of Figure 2). The resulting impedance is the impedance needed to exceed the combination of the template and the 100-ohm termination.

b) When transmitting a binary ZERO, the output impedance shall be ≥ 20 ohms.

NOTE – The output impedance limit shall apply for a nominal load impedance (resistive) of 50 ohms. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ±10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

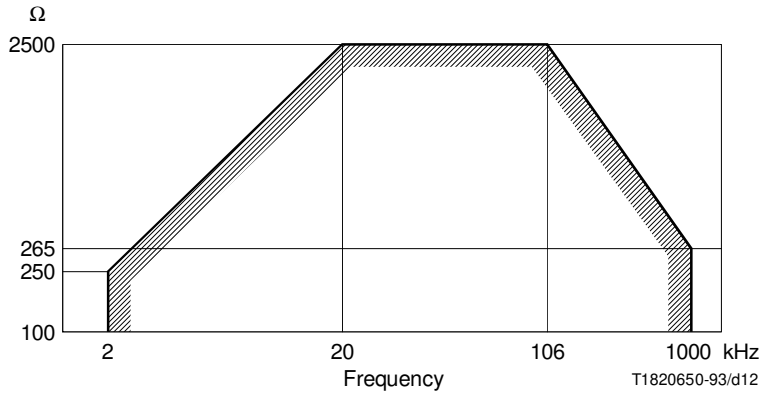


FIGURE 11/I.430

NT impedance template (log-log scale)

8.5.1.2 TE transmitter output impedance

a) At all times except when transmitting a binary ZERO, the following requirements apply:

i) The output impedance, in the frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated by the template in Figure 12. This requirement is applicable with applied sinusoidal voltage of 100 mV (r.m.s. value).

ii) At a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 0.6 mA (peak value).

b) When transmitting a binary ZERO, the output impedance shall be ≥ 20 ohms.

NOTE – The output impedance limit shall apply for two nominal load impedance (resistive) conditions: 50 ohms and 400 ohms. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ±10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

8.5.2 Test load impedance

The test load impedance shall be 50 ohms (unless otherwise indicated).

8.5.3 Pulse shape and amplitude (binary ZERO)

8.5.3.1 Pulse shape

Except for overshoot, limited as follows, pulses shall be within the mask of Figure 13. Overshoot, at the leading edge of pulses, of up to 5% of the pulse amplitude at the middle of a signal element, is permitted, provided that such overshoot has, at 1/2 of its amplitude, a duration of less than 0.25 μs.

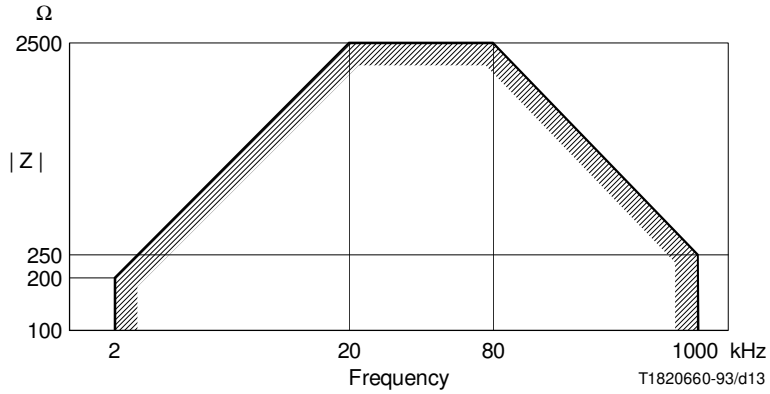
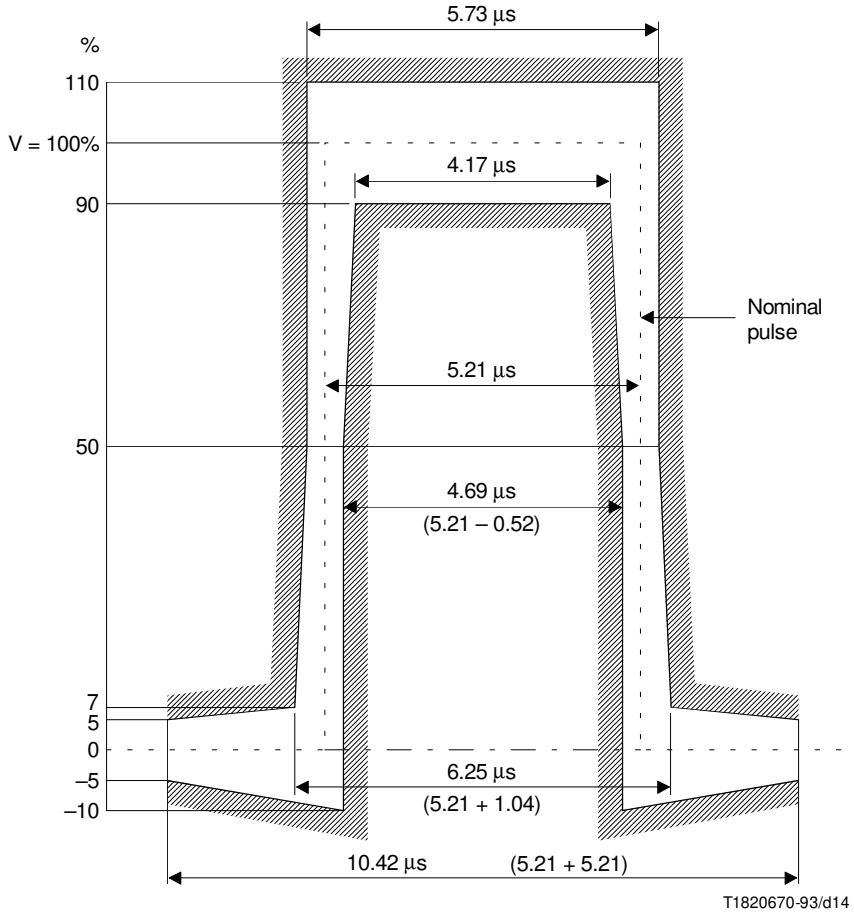


FIGURE 12/I.430

TE impedance template (log-log scale)



NOTE – For clarity of presentation, the above values are based on a pulse width of 5.21 µs. See 8.1 for a precise specification of the bit rate.

FIGURE 13/I.430

Transmitter output pulse mask

8.5.3.2 Nominal pulse amplitude

The nominal pulse amplitude shall be 750 mV, zero to peak.

A positive pulse (in particular, a framing pulse) at the output port of the NT and TE is defined as a positive polarity of the voltage measured between access leads e to f and d to c respectively (see Figure 21). (See Table 12 for the relationship to connector pins.)

8.5.4 Pulse unbalance

The "pulse unbalance", i.e. the relative difference in $\int U(t)dt$ for positive pulses and $\int U(t)dt$ for negative pulses shall be $\leq 5\%$.

8.5.5 Voltage on other test loads (TE only)

The following requirements are intended to assure compatibility with the condition where multiple TEs are simultaneously transmitting pulses on a passive bus.

8.5.5.1 400-ohm load

A pulse (binary ZERO) shall conform to the limits of the mask shown in Figure 14 when the transmitter is terminated in a 400-ohm load.

8.5.5.2 5.6-ohm load

To limit the current flow with two drivers having opposite polarities, the pulse amplitude (peak) with a 5.6-ohm load shall be $\leq 20\%$ of the nominal pulse amplitude.

8.5.6 Unbalance about earth

The following requirement applies under all possible power feeding conditions, under all possible connections of the equipment to ground, and with two 100-ohm terminations across the transmit and receive ports.

Longitudinal conversion loss (LCL) which is measured in accordance with 4.1.3/G.117 (see Figures 15 and 16), shall meet the following requirements:

a) 10 kHz $\leq f \leq$ 300 kHz: $\geq$ 54 dB

b) 300 kHz $< f \leq$ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.

8.6 Receiver input characteristics

8.6.1 Receiver input impedance

8.6.1.1 TE receiver input impedance

TEs shall meet the same input impedance requirements as specified in 8.5.1.2 a), i) and ii) for the output impedance, independently of the state of the terminal (F1 to F8).

8.6.1.2 NT receiver input impedance

a) NT without internal terminating resistor

   At all times, the following requirements apply:

   i) the input impedance in the frequency range of 2 kHz to 1 MHz should exceed the impedance indicated by the template in Figure 11. This requirement is applicable with an applied sinusoidal voltage of 100 mV (r.m.s. value);

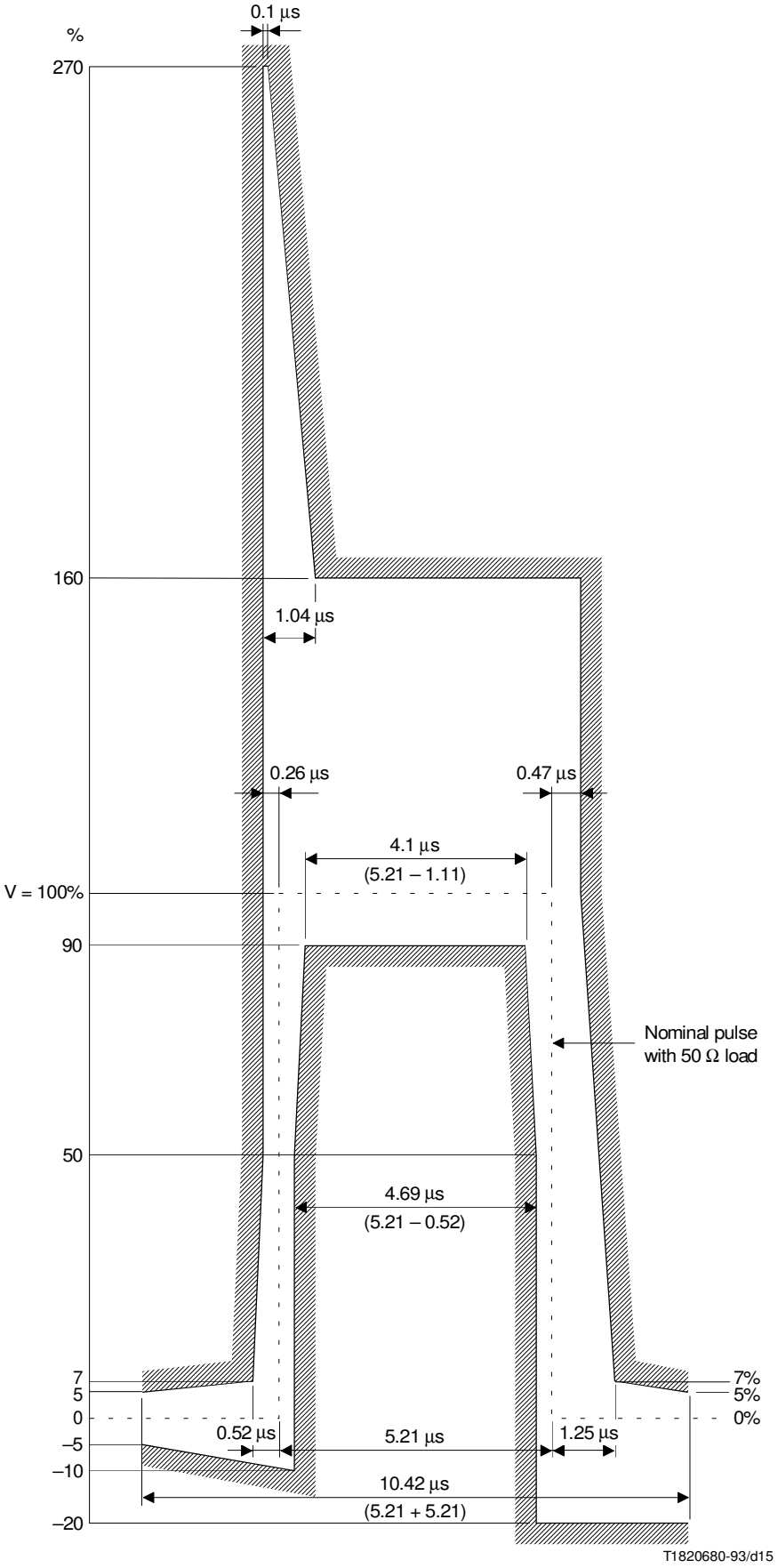
   ii) at a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 0.5 mA (peak value).

b) NT with internal 100-ohm terminating resistor (see point B of Figure 2)

   At all times, the following requirements apply:

   i) the input impedance in the frequency range of 2 kHz to 1 MHz should exceed the combination of the 100-ohm resistor plus the impendance indicated by the template in Figure 11. This requirement is applicable with an applied sinusoidal voltage of 100 mV (r.m.s. value);

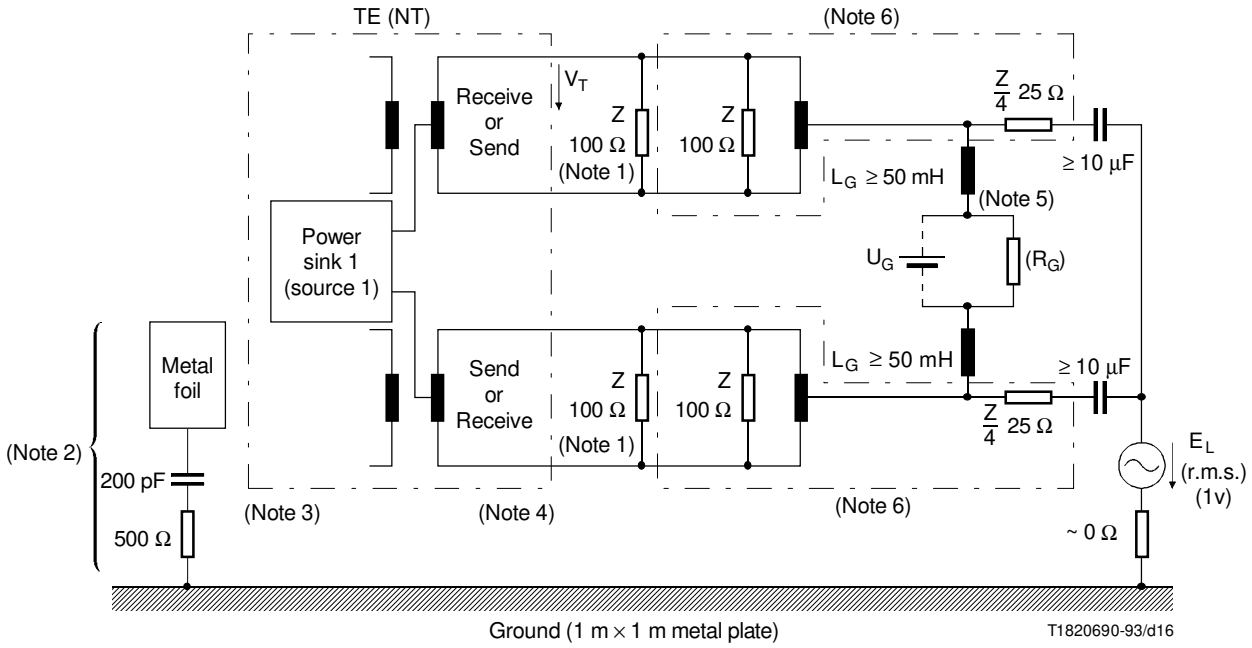
   ii) at a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1.2 V (peak value) should not exceed 13 mA (peak value).



NOTE – For clarity of presentation, the above values are based on a pulse width of 5.21 µs. See 8.1 for a precise specification of the bit rate.

FIGURE 14/I.430

Voltage for an isolated pulse with a test load of 400 ohms



The longitudinal conversion loss: $LCL = 20 \log_{10} \left| \frac{E_L}{V_L} \right|$ dB.

The voltages V_T and E_L should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment.

The measurement should be carried out in the states:

– deactivated (receive, send);

– power off (receive, send);

– activated (receive).

The interconnecting cord shall lie on the metal plate.

NOTES

1 This resistor must be omitted if the termination is already built into the TE (NT).

2 Hand imitation is a thin metal foil, approximately the size of a hand.

3 TE (NT) with a metallic housing shall have a galvanic connection to the metal plate. Other TE (NT) with non-metallic housing shall be placed on the metal plate.

4 The power cord for mains-powered TE (NT) shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.

5 If there is no power source 1 in the NT, R_G and L_G are not required.

6 This circuit provides a transverse termination of 100 ohms and a balanced longitudinal termination of 25 ohms. Any equivalent circuit is acceptable. However, for equivalent circuits given in Recommendations G.117 and O.121, powering cannot be provided.

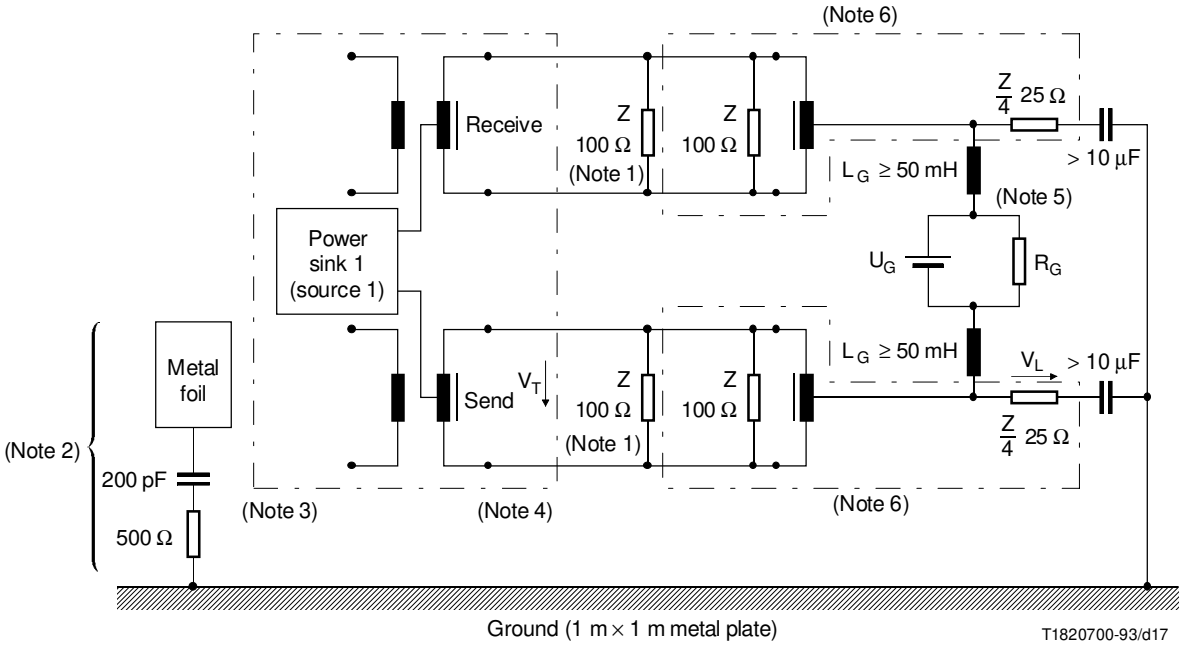
FIGURE 15/I.430

Receiver input or transmitter output unbalance about earth

8.6.2 Receiver sensitivity – Noise and distortion immunity

Requirements applicable to TEs and NTs for three different interface wiring configurations are given in the following subclauses. TEs and/or NTs shall receive, without errors (for a period of at least one minute), an input with a pseudo-random sequence (word length ≥511 bits) in all information channels (combination of B-channel, D-channel and, if applicable, the D-echo channel).

The receiver shall operate, with any input sequence, over the full range indicated by the waveform mask.



Output signal balance = $20 \log_{10} \left| \frac{V_T}{V_L} \right|$ dB.

The voltages V_T and V_L should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment. The measurement should be carried out in the activated states. The pulse patterns should contain all binary ZEROs. However, for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure the output signal unbalance about earth with a pulse pattern of continuous frames with at least the B1 and B2 channels containing all binary ZERO's.

The interconnecting cord shall lie on the metal plate.

NOTE – Notes 1 to 6 of Figure 15 are also applicable in this case.

FIGURE 16/I.430

Transmitter output unbalance about earth

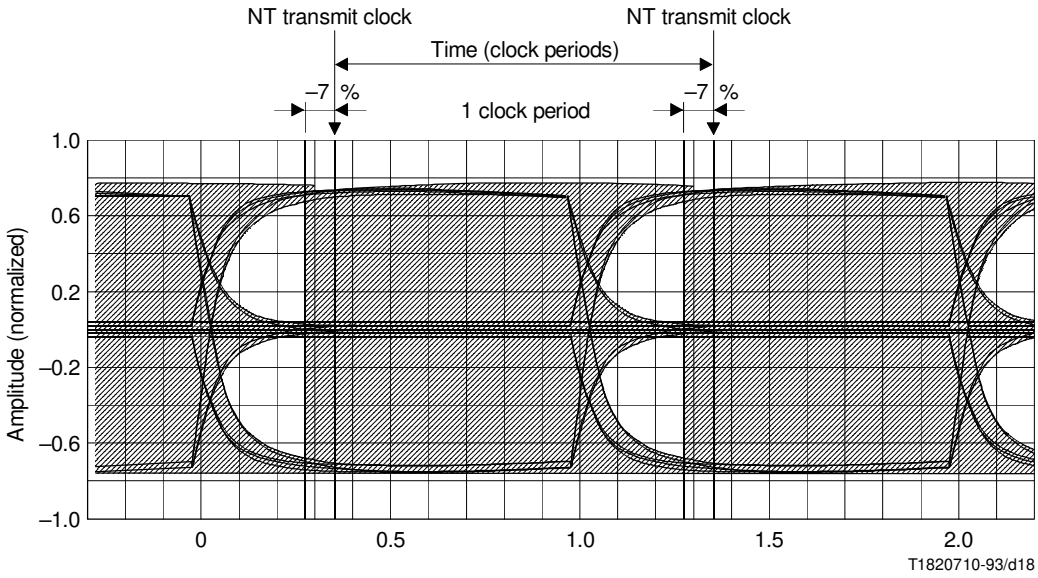
8.6.2.1 TEs

TEs shall operate with the input signals conforming to the waveforms specified in 8.2.1. For the waveforms in Figures 7 to 9, TEs shall operate with the input signals having any amplitude in the range of +1.5 dB to –3.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2. For signals conforming to the waveform in Figure 6, operation shall be accomplished for signals having any amplitude in the range of +1.5 to –7.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2. In addition, TEs shall operate with signals conforming to each waveform with jitter up to the maximum permitted (see 8.3) in the output signal of NTs superimposed on the input signals.

Additionally, for input signals having the waveform shown in Figure 6, the TEs shall operate with sinusoidal signals having an amplitude of 100 mV (peak-to-peak value) at frequencies of 200 kHz and 2 MHz superimposed individually on the input signals along with jitter.

8.6.2.2 NTs for short passive bus (fixed timing)

NTs designed to operate with only short passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 17. NTs shall operate, with the input signals having any amplitude in the range of +1.5 dB to –3.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2.



NOTES

1 Shaded area is the region in which pulse transitions may occur.

2 The waveform mask is based on the "worst case" configuration shown in Annex D. Figure D.1 and waveforms ii) and iii) in 8.2.1. The shaded area of –7% of one clock period accounts for the situation of a single TE connected directly to the NT with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and D-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 17/I.430

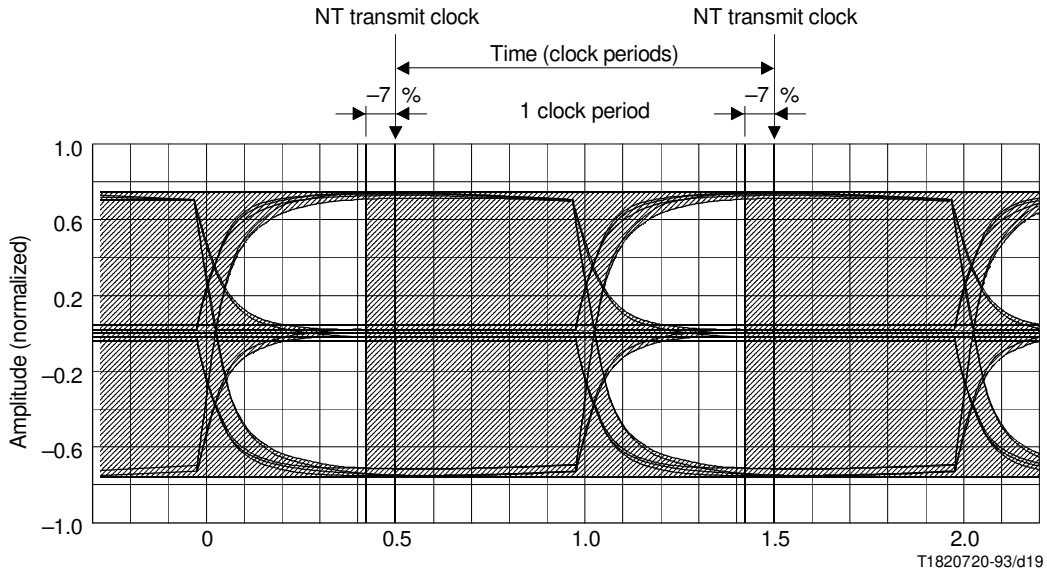
Short passive bus receive pulse waveform mask

8.6.2.3 NTs for both point-to-point and short passive bus configurations (adaptive timing)

NTs designed to operate with either point-to-point or short passive wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 18. These NTs shall operate with the input signals having any amplitude in the range of +1.5 dB to −3.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2. These NTs shall also operate when receiving signals conforming to the waveform in Figure 6. For signals conforming to this waveform, operation shall be accomplished for signals having any amplitude in the range of +1.5 to −7.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2. Additionally, these NTs shall operate with the sinusoidal signals, as specified in 8.6.2.1, and with jitter up to the maximum permitted in the output signal of TEs (see 8.2.2), superimposed on the input signals having the waveform in Figure 6.

8.6.2.4 NTs for extended passive bus wiring configurations

NTs designed to operate with extended passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in Figure 19. These NTs shall operate with the input signals having any amplitude in the range of +1.5 dB to −5.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2. Additionally, these NTs shall operate with the sinusoidal signals, as specified in 8.6.2.1, superimposed on the input signals having the waveform shown in Figure 19. (The above values assume a maximum cable loss of 3.8 dB. NTs may be implemented to accommodate higher cable loss.)



NOTES

1 Shaded area is the region in which pulse transitions may occur.

2 The waveform mask is based on the same "worst case" passive bus configuration as the waveform mask in Figure 17 except that the permitted round trip delay of the cable is reduced. The shaded area of –7% of one clock period accounts for the situation of a single TE connected directly to the NT with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and D-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 18/I.430

Passive bus receive pulse waveform mask (NTs designed to operate with either point-to-point or short passive bus wiring configurations)

8.6.2.5 NTs for point-to-point configurations only

NTs designed to operate with only point-to-point wiring configurations shall operate when receiving input signals having the waveform shown in Figure 6. These NTs shall operate with the input signals having any amplitude in the range of +1.5 dB to −7.5 dB relative to the nominal amplitude of the transmitted signal as specified in 8.5.3.2. Additionally, these NTs shall operate with the sinusoidal signals, as specified in 8.6.2.1, and with jitter up to the maximum permitted in the output signal of TEs (see 8.2.2) superimposed on the input signals having the waveform shown in Figure 6.

8.6.3 NT receiver input delay characteristics

NOTE – Round trip delay is always measured between the zero-volt crossings of the framing pulse and its associated balance bit pulse at the transmit and receive side of the NT (see also Annex A).

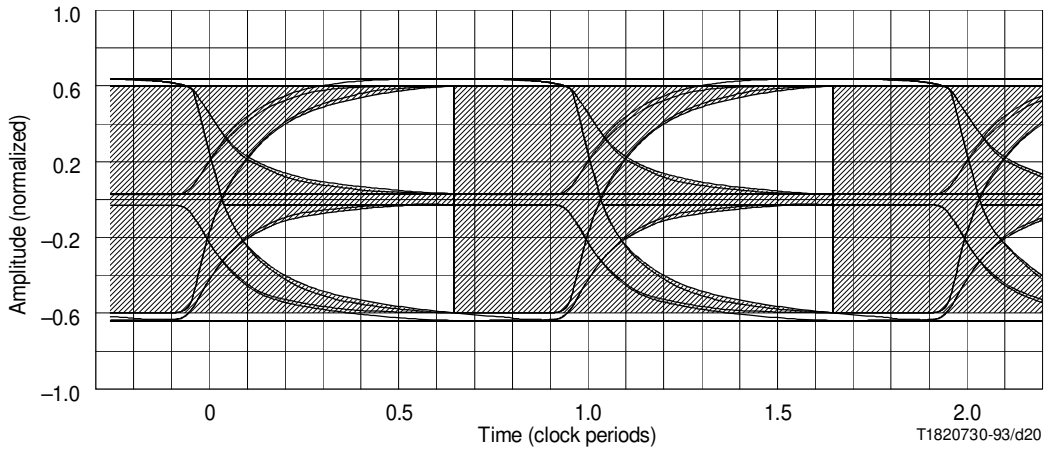
8.6.3.1 NT for short passive bus

NTs shall accommodate round trip delays of the complete installation, including TEs, in the range 10 to 14 μs.

8.6.3.2 NT for both point-to-point and passive bus

NTs shall accommodate round trip delays (for passive bus configurations) in the range 10 to 13 μs.

NTs shall accommodate round trip delays (for point-to-point configurations) in the range 10 to 42 μs.



NOTES

1 Shaded area is the region in which pulse transitions may occur.

2 The waveform mask is based on the "worst case" extended passive bus wiring configuration. It consists of a cable having a characteristic impedance of 75 ohms, a capacitance of 120 nF/km, a loss of 3.8 dB at 96 kHz, four TEs connected such that the differential delay is at the maximum permitted by 8.6.3.3. The waveform mask does not show the higher possible amplitude of framing and D-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

FIGURE 19/I.430

Extended passive bus receive pulse waveform mask

8.6.3.3 NT for extended passive bus

NTs shall accommodate round trip delays in the range 10 to 42 μs, provided that the differential delay of signals from different TEs is in the range 0 to 2 μs.

8.6.3.4 NT for point-to-point only

NTs shall accommodate round trip delays in the range 10 to 42 μs.

8.6.4 Unbalance about earth

Longitudinal conversion loss (LCL) of receiver inputs, measured in accordance with 4.1.3/G.117, by considering the power feeding and two 100-ohm terminations at each port, shall meet the following requirements (see Figure 15):

a) 10 kHz ≤ f ≤ 300 kHz: ≥ 54 dB

b) 300 kHz < f ≤ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.

8.7 Isolation from external voltages

IEC Publication 479-I, Second Issue 1984, specifies current limitations dealing with human safety. According to that publication, the value of a touchable leakage alternating current measured through a resistor of 2 kohms is limited. The application of this requirement to the user-network interface is not a subject of this Recommendation, but it should be recognized that an apportionment of this limited current to each mains power equipment connected to the passive bus is necessary.

8.8 Interconnecting media characteristics

Interface cables (or cabling) shall include twisted metallic pairs (two up to four as required). Such pairs will frequently be part of the customers' premises distribution systems. The transmission characteristics of the transmit and receive pairs shall be such that satisfactory operation is assured when used to interconnect (I_A to I_B) equipment having interfaces conforming to the requirements of this Recommendation. Examples of cable system parameters that must be considered are loss, frequency response crosstalk loss, longitudinal balance and noise. Note that cable characteristics assumed in defining the requirements specified in this Recommendation at interface point I_A and I_B are discussed in Annex A and Table D.1. Longitudinal balance, e.g. > 43 dB at 96 kHz, is of particular importance in assuring compliance with EMI limitations which must also be considered in determining suitable interface cables.

8.9 Standard ISDN basic access TE cord

A connection cord for use with a TE designed for connection with a "standard ISDN basic access TE cord" shall have a maximum length of 10 metres and shall conform to the following:

a) *Cords having a maximum length of 7 metres*

- the maximum capacitance of pairs for transmit and receive functions shall be less than 300 pF;
- the characteristic impedance of pairs used for transmit and receive functions shall be greater than 75 ohms at 96 kHz;
- the crosstalk loss, at 96 kHz, between any pair and a pair to be used for transmit or receive functions shall be greater than 60 dB with terminations of 100 ohms;
- cords shall be terminated at both ends in identical plugs (individual conductors shall be connected to the same contact in the plug at each end);
- the resistance of an individual conductor (including the connector pins at each end) shall not exceed 3.2 ohms (including the permissible tolerance) and the difference in the resistance of conductors of a pair shall not exceed 6% or 60 mohms, whichever is greater.

b) *Cords having a length greater than 7 metres*

- cords shall conform to the above requirements except that a capacitance of 350 pF is permitted.

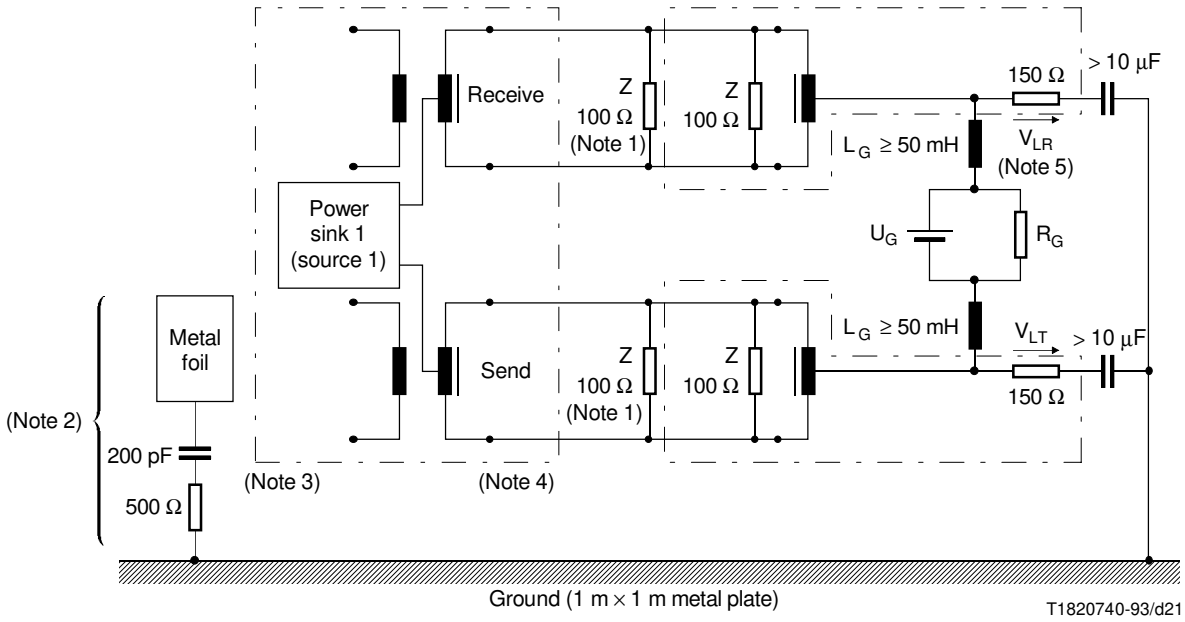
TEs may be designed that include a connecting cord which is part of the TE. In this case the requirements for a standard ISDN basic access TE cord do not apply.

8.10 Longitudinal output voltage

The longitudinal voltage of receivers and transmitters in the frequency band of 10 kHz to 150 kHz shall be limited, as follows, when measured across a longitudinal termination of 150 ohms as shown in Figure 20.

8.11 Electromagnetic compatibility (EMC)

The electrical characteristics specified within this Recommendation do not in themselves guarantee that electromagnetic compatibility will be achieved with other user premises equipment, systems or with applicable EMC regulations. A Recommendation in the K-Series refers to these characteristics.



V_{LT} and $V_{LR} \leq -24$ dBV peak.

V_{LT} and V_{LR} shall be measured when NT sends INFO 2 and TE sends INFO 1.

The measured bandwidth shall be 3 kHz.

NOTE – Notes 1 to 5 of Figure 15 are also applicable in this case.

FIGURE 20/I.430

Longitudinal voltage of receivers and transmitter

9 Power feeding

9.1 Reference configuration

The reference configuration for power feeding, which is based on an eight pin interface connector, is described in Figure 21. The access lead designations, "a" through "h", are not intended to reflect particular pin assignments, which as indicated in 10, are specified in ISO 8877. The use of leads c, d, e, and f is mandatory. The use of leads a, b, g and h is optional.

This reference configuration allows unique physical and electrical characteristics, for the interface at reference points S and T, which are independent of the choice of internal or external power source arrangements.

Power source 1 may derive its power from the network and/or locally (mains and/or batteries). Three possible power source arrangements have been considered:

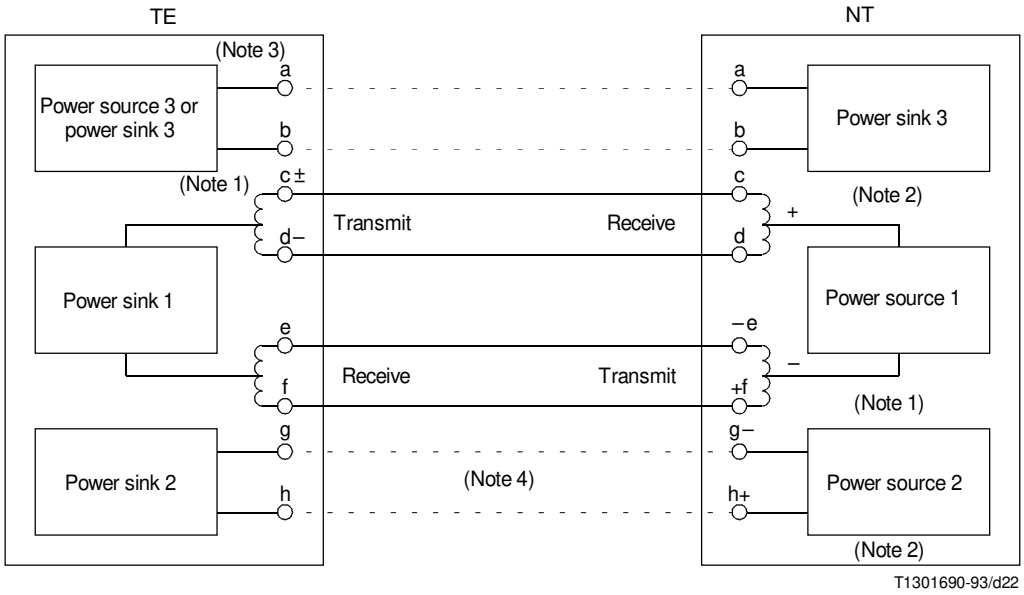
1) The sources for restricted mode and normal mode power are both integral to the NT.

2) The source for restricted mode power is an integral part of the NT, while the source for normal mode may be physically separate and may be connected at any point in the interface wiring. In this case, the source is referred to as an auxiliary power source (APS). Note that such an APS should be considered functionally part of the NT. However, the provision of an APS is subject to the approval of the Administration/network provider. To avoid interworking problems, it is not permitted to connect an APS in wiring associated with NTs having an internal source for normal mode. Where an APS is provided, its compatibility with a source for restricted mode that is part of the associated NT must be assured by the

provider of the APS. In particular, the resolution of power contention, which may result from the provision of the APS, between the APS and a restricted mode source internal to an NT, must be taken into account (refer to 9.9 and 9.10). In addition, the effects on the transmission characteristics of interface cabling must also be accounted for, eg. the impedance of an APS that bridges the interchange circuit pairs may require a reduction in the number of TEs that can be accomodated on a passive bus.

3) The source for normal mode power is an integral part of the NT while the source for restricted mode power may be physically separate and may be connected at any point in the interface wiring. To avoid interworking problems in this case, it is not permitted to connect a source providing restricted mode power in wiring associated with an NT having an internal source of restricted mode power. The requirements for the normal mode source in the NT are the same as those for an APS (refer to 9.9), while the requirements for the restricted mode source designed to be connected at any point in the interface wiring are the same as those for a restricted mode source which interworks with an APS (refer to 9.10).

Power source 2 derives its power locally (mains and/or batteries). Power source 2 may be located in (or associated with) the NT as indicated, or it may be located separately.



NOTES

1 This symbol refers to the polarity of framing pulses.

2 This symbol refers to the polarity of power during normal power conditions (reversed for restricted conditions).

3 The access lead assignments indicated in this figure are intended to provide for direct interface cable wiring, i.e. each interface pair is connected to a pair of access leads having the same two letters at TEs and NTs.

4 If access pair g-h is used for PS2 power feeding, the polarity of wires within this pair must be maintained, i.e. the wires must not be interchanged.

FIGURE 21/I.430

Reference configuration for signal transmission and power feeding in normal operating mode

9.1.1 Functions specified at the access leads

The eight access leads for TE and NT shall be applied as follows:

i) Access lead pairs c-d and e-f are for the bidirectional transmission of the digital signal and may provide a phantom circuit for power transfer from NT to TE (power source 1);

ii) Access lead pair g-h may be used for additional power transfer from the NT to TE (power source 2);

iii) Access lead pair a-b may also be used for power transfer in TE-TE interconnection and power transfer from TE to NT (power source 3).

9.1.2 Provision of power sources and sinks

– *Power feeding in the direction NT to TE*

Power sources 1 and 2 allow for power feeding in the direction NT to TE. Power source 1 (phantom power) may not always be provided. Provision of power source 2 is subject to the decision of individual Administrations. Power sink 1 is optional. Administrations may limit the use of power from power source 1 to those TEs capable of providing a minimum service. Power sink 2 is optional. Power source 2 is intended as an alternative to power source 1, and normally both power sources would not be provided in the same network.

NOTE – It should be noted that a TE that is to be portable (for example from network to network, country to country) cannot rely exclusively on phantom power for its operation.

– *Power feeding in the direction TE to NT and TE to TE*

Power source 3 allows for the possibility of power feeding in the direction TE to NT or TE to TE. Power source 3 is not subject to CCITT Recommendation. However, it must be noted that, since a TE is allowed to contain either a power source 3 or a power sink 3 (refer to Table 12), TE to TE power feeding using power source 3 requires special care to avoid possible power contention issues. See Figure 21.

9.1.3 Power feeding voltage

Requirements for power feeding are given for a basic voltage range of 34 V to 42 V from the power source. For some networks (for example, PBX), a higher maximum voltage of 56.5 V is desirable to allow compatibility with 48 V power sources used for other purposes.

In the following detailed requirements for TEs and power sources, (see 9.2.2, 9.2.3, 9.3.2, 9.3.3), the voltage limits given are for the basic range, with the values for the optional increased voltage range in parentheses.

NOTES

1 Although all TEs must meet at least the basic voltage range requirements, a TE which is intended to be fully portable must be designed to meet all performance parameters over the increased voltage range.

2 For power sources having an output voltage greater than 42 V, there is a need to provide additional transient capability to ensure proper interworking with all TEs (see 9.7.4.2).

3 Throughout this Recommendation, all the values referring to power in watts (or in PCU) shall be measured using an instrument which integrates the measurements over a period of 50 ms.

9.2 Power available from NT

9.2.1 Power source 1 normal and restricted mode

Power source 1 may provide either normal or restricted mode or both.

i) Where power is provided under normal mode, the power available from power source 1 is the responsibility of the individual Administration/network provider. However, power source 1 together with any separate power source as described in 9.1, shall provide at least 10 power consumption units (normal) at a TE interface. The power required to be available at the source will depend on the interface cable configuration. (power consumption units (PCU) are defined in 9.3.1.)

ii) Under restricted mode, the minimum power available from power source 1 shall be 420 mW. When power source 1 enters a condition where it is able to supply only restricted power, it should indicate this condition by reversing its polarity. In this condition, only the restricted power functions of TEs are allowed to consume power from power source 1.

iii) If power source 1 (and any separate source combination) can supply power in both normal and restricted modes, the change of condition of power source 1 from the normal to restricted mode may occur when power source 1 (and any separate source combination) is unable to supply the "nominal" level of power. (The "nominal" level of power is defined as the minimum power that the power source 1 (or separate power source) is designed to supply.) In any case, the transition from normal to restricted mode shall occur when the power described in 9.2.1 i) is not available from power source 1 (as a result of a loss of its source of power).

iv) If the PS1 source loses its primary power, it may switch to restricted mode as an option to conserve secondary power, even though it may still be capable of supplying its full rated normal power output.

9.2.2 Voltage NT from power source 1

9.2.2.1 Normal mode

Under normal mode, the voltage of power source 1, if provided, at the output of the NT shall be within the range 34 V to 42 V (Optionally 56.5 V; see 9.1.3) when supplying up to the maximum available power.

9.2.2.2 Restricted mode

Under restricted mode, the voltage of power source 1, if provided, at the output of the NT shall be within the range 34 V to 42 V (optionally 56.5 V; see 9.1.3) when supplying up to its rated maximum power, which shall be not less than 420 mW.

9.2.3 Voltage of power source 2

The maximum voltage of power source 2 (optional third pair) shall be 42 V (optionally 56.5 V; see 9.1.3) and the minimum voltage shall assure compliance with the requirements specified in 9.3.2 concerning power available at a TE.

9.2.4 Short circuit protection

Power sources shall provide short-circuit protection. This requirement may be checked by applying a short-circuit for a period of 30 minutes, after which the power source shall be able to provide its rated PCUs within 10 seconds (60 seconds in the case of interface at the S-reference point). Verification of compliance may be combined with the test described in 9.7.4.

9.3 Power available at TE

9.3.1 Power consumption unit

The power which a TE is designed to draw from power source 1 or 2 should be given in terms of "power consumption units". For normal mode, one power consumption unit (NPCU) shall be equivalent to 100 mW, while for restricted mode, one power consumption unit (RPCU) shall be equivalent to 95 mW. (The difference in units is required to allow adequate margins for power consumed by non-designated terminals in restricted mode.) Fractional PCU values are not allowed, i.e. actual TE power consumption shall be rounded up to the next integer value. The PCU rating of a TE shall be applicable over the full range of specified operating voltage, and shall represent the maximum power drawn by that TE at any voltage within this range.

NOTE – The use of power consumption units (to define power consumed by the TE and power available from the source) does not imply any lack of backward compatibility with TEs and/or power sources designed in accordance with the requirements given in the *Blue Book* version of Recommendation I.430. A TE or PS1 power source designed to meet those requirements has a rating of 10 NPCUs (normal mode) and 4 RPCUs (restricted mode).

The power that a PS1/PS2 source is designed to provide shall also be given in terms of PCUs, NPCU for normal mode and RPCU for restricted mode. The total PCUs available in this case takes account of the power loss in the loop resistance of the cabling configuration(s) for which the power source is designed, and represents the power available for

the TEs to draw. Note that this may mean that the same power source may, as an option, be given different PCU ratings for different cable configurations (for example, one rating for point-to-point, and a different rating for point-to-multipoint).

A TE may be designed to draw any number of PCUs from power source 1 or 2, up to a maximum of 80 NPCU for normal mode. In restricted mode, the maximum that a TE may be designed to draw is 4 RPCU for PS1, and 21 RPCU for PS2.

For a given installation, the sum of the NPCU ratings for all TEs on a bus must not exceed the NPCU rating of the power source (PS1 or PS2, as applicable). Similarly, the sum of the RPCU ratings for all designated TEs on a bus must not exceed the RPCU rating of the power source. In either case, the connection of TEs with a total PCU rating exceeding the corresponding PCU rating of the respective power source may disrupt operation of all TEs on the bus.

9.3.2 Power source 1 – Phantom powering

9.3.2.1 Normal mode

Under normal mode, the maximum voltage at the interface of a TE shall be 42 V (optionally 56.5 V; see 9.1.3) and the minimum voltage shall be 24 V when drawing up to the designed maximum available NPCUs.

9.3.2.2 Restricted mode

In restricted mode, the maximum value of the voltage at the interface of a TE (from power source 1) shall be 42 V (optionally 56.5 V; see 9.1.3) and the minimum voltage shall be 32 V when drawing a power of up to 400 mW (4 RPCU for designated TEs and 20 mW for other TEs). The power source may, as an option, be designed to provide more than 4 RPCUs. If so, the voltage shall be within the limits given when the TEs are drawing up to the designed maximum available RPCUs.

9.3.3 Power source 2 – Optional third pair

9.3.3.1 Normal mode

Under normal mode, the voltage at the interface of a TE shall be a maximum of 42 V (optionally 56.5 V; see 9.1.3) and a minimum of 32 V when the TE is drawing a power of up to 80 NPCUs.

9.3.3.2 Restricted mode

The provision of the restricted mode is subject to the power source 2 provider's assumed responsibility.

When power source 2 is unable to provide the designed NPCUs for normal mode, it goes to a restricted mode (indicated by reversing its polarity) in which it shall provide a minimum of 21 RPCUs. The maximum voltage at the inputs of the TEs shall be 42 V (optionally 56.5 V; see 9.1.3) and the minimum shall be 32V when drawing a power of up to 21 RPCUs. The power source may, as an option, be designed to provide more than 21 RPCUs. If so, the voltage shall be within the limits given when the TEs are drawing up to the designed maximum available RPCUs.

If the PS2 source loses its primary power, it may switch to restricted mode as an option to conserve secondary power, even though it may still be capable of supplying its full rated normal power output.

9.4 PS1 current transient

The rate of change of current drawn by a TE from power source 1 shall not exceed 5 mA/μs.

NOTE – This does not apply for the first 100 ms after connection, or after a change in polarity when a change from the normal mode to the restricted mode occurs. Also, if the revised current/time mask suggested in Appendix II, (see II.7.1) is used, the 100 ms period is delayed by the time "B" given in Table II.2.

9.5 TE power consumption

9.5.1 Power source 1

The different values concerning the TE PS1 consumption are summarized in Table 11.

TABLE 11/I.430

Summary of the different possible TE PS1 consumptions

TE type and state	Maximum consumption
Normal mode	
TE drawing power from PS1 Activated state	Rated NPCU (Note 1)
TE drawing power from PS1 Deactivated state	100 mW
TE Drawing power from PS1 Local action state	(Note 2) Rated NPCU (Note 1)
Restricted mode	
TE drawing power from PS1 Designated TE: Activated state	Rated RPCU (Note 3)
TE drawing power from PS1 Designated TE: Deactivated state	25 mW
TE drawing power from PS1 Not designated	0 mW
TE drawing power from PS1 Designated: Local action state	(Note 2) Rated RPCU (Note 3)
TE not powered from PS1 but using connected detector on PS1: Any state	3 mW
TE not powered from PS1 and not using a connected detector: Any state	0 mW
NOTES 1 Rated NPCU not to exceed 80. Refer to 9.3.1. For rated NPCU greater than 10, TE portability is not guaranteed even where PS1 is provided. Refer to 9.2.1. 2 Subject to the provision of the corresponding amount of power by power source 1. 3 Rated RPCU not to exceed 4. Refer to 9.3.1.	

9.5.1.1 Normal mode

Under normal mode and in the activated state, a TE that draws power from power source 1 shall draw no more than its rated NPCUs, which shall not exceed 80, from power source 1. When a TE is not involved in a call, it is desirable that it minimize its power consumption (see Note below).

When in the deactivated state, a TE that draws power from power source 1 shall draw no more than 100 mW. However, if a local action has to be initiated in the TE when the interface is not activated, this TE shall enter a “local action” state.

In this "local action" state, the TE may consume up to its rated NPCUs, if the following conditions are assured:

i) The corresponding power is provided by the NT (e.g. this service is supported by the NT).

ii) The "local action" state is not a permanent one. (A typical example of the use of this state is the modification of prestored dialling numbers in the TE).

NOTE – The definition of "not involved in a call" mode may be based on the knowledge of the status of layer 2 (link established or not). When this limitation is applied in the design of a TE, a maximum value of 380 mW is recommended.

9.5.1.2 Restricted mode

9.5.1.2.1 Power available to a TE "designated" for restricted power operation

A TE which is permitted to draw power from power source 1 under restricted mode shall consume no more than 4 RPCUs. In restricted mode, a designated TE which is powered down may consume power from power source 1 only to maintain a line activity detector and to retain its terminal endpoint identifier (TEI) value. The value of the power down mode consumption shall not exceed 25 mW.

9.5.1.2.2 Power available to other TEs

TEs, not powered by PS1, which make use of a PS1 connected/disconnected detector may consume no more than 3 mW from power source 1 in restricted mode.

TEs, not powered by PS1, which do not make use of a connected/disconnected detector and non-designated TEs which are normally powered from power source 1 (normal mode) shall not consume any power from power source 1 in restricted mode (except the leakage current as defined in 9.7.1.1).

9.5.2 Power source 2

9.5.2.1 Normal mode

Under normal mode and in the activated state, a TE that draws power from power source 2 shall draw no more than its rated NPCUs, which shall not exceed 80, from power source 2. When a TE is not involved in a call, or when it is in the deactivated state, it is desirable that it minimize its power consumption (see Note below). However, if a local action has to be initiated in the TE when the interface is not activated, this TE shall enter a "local action" state and may consume up to its rated NPCUs.

NOTE – The definition of "not involved in a call" mode may be based on the knowledge of the status of layer 2 (link established or not). When this limitation is applied in the design of a TE, a maximum value of 2 W is recommended.

9.5.2.2 Restricted mode

9.5.2.2.1 Power available to a TE "designated" for restricted power operation

A TE which is permitted to draw power from power source 2 under restricted mode shall consume no more than 21 RPCUs. In restricted mode, a designated TE which is powered down may consume power from power source 2 only to maintain a line activity detector and to retain its terminal endpoint identifier (TEI) value. The value of the power down mode consumption shall not exceed 200 mW.

9.5.2.2.2 Power available to other TEs

TEs, not powered by PS2, and non-designated TEs which are normally powered from power source 2 (normal mode) shall not consume any power from power source 2 in restricted mode (except the leakage current as defined in 9.7.1.2).

9.6 Galvanic isolation

TEs shall provide galvanic isolation between power source 1/2 and the earths of additional sources of power and/or of other equipment. Isolation shall be a minimum of 1 Mohm when measured at 500 V DC between an interface conductor and any one of the following points: AC mains earth; all pins of any external interfaces; or any conductive

surface. Equipment must also comply with the applicable IEC safety specifications. (This provision is intended to preclude earth loops or paths which could result in currents that would interfere with the satisfactory operation of the TE. It is independent of any requirement, for such isolation, related to safety which may result from the study under way in IEC-ACOS/TES.)

9.7 Limitations on power source and sink during transient condition

NOTE – Throughout 9.7, the following definitions apply:

– maximum number of TEs to be fed via the interface = n;

– maximum number of these n TEs which are designated = m;

– designed NPCUs for a given TE = N;

– designed RPCUs for a given TE = M;

– total NPCUs consumed by all TEs on bus = p;

– total RPCUs consumed by all TEs on bus = q;

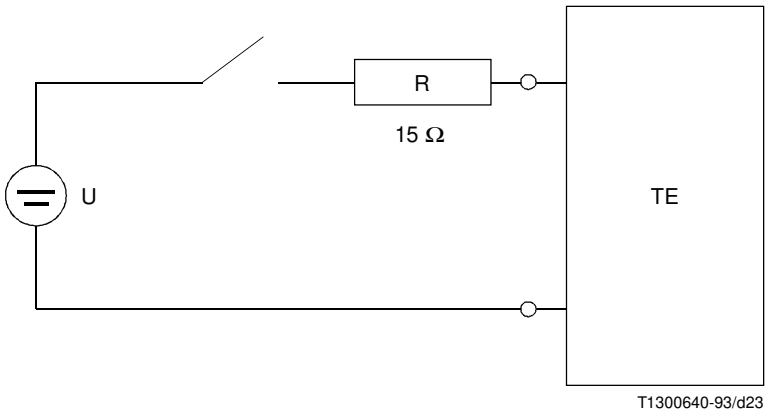
– rated NPCUs of power source = P;

– rated RPCUs of power source = Q.

9.7.1 Current/time limitations for TEs

9.7.1.1 Terminals powered from power source 1

To limit the current that each terminal can sink from the phantom circuit when connected to PS1 in normal mode, or when PS1 changes from restricted to normal mode, the terminal shall conform to the mask given in Figure 23 with the values given in Table 12, when tested in accordance with Figure 22.



U Voltage source, 40 V

FIGURE 22/I.430

Test circuit to Figure 23/I.430

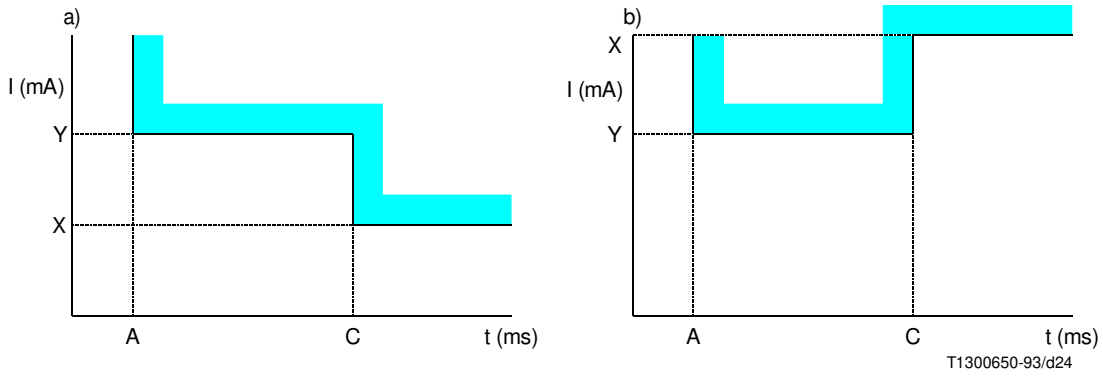


FIGURE 23/I.430

Current/Time limitation for TE

TABLE 12/I.430

PS1 Parameters for TE in normal mode

A	5 µs
Y	55 mA or, for N < 10, (N × 5,5)mA
C	100 ms
X	Current equivalent to NPCU of TE
N NPCUs drawn by TE	

NOTE – As an alternative, it is acceptable to delay the current surge by up to 900 ms after connection to PS1, or when PS1 changes from normal to restricted mode. Refer to Appendix II for current-time mask revised to accomodate this option.

Diagram a) of Figure 23 is drawn to illustrate a typical terminal. For some high-power terminals (power consumption greater than approximately 22 NPCUs), the current X will be greater than the current Y, as shown in diagram b) of Figure 23.

To limit the current that a designated terminal can sink from the phantom when connected to PS1 in the restricted condition, a designated terminal shall conform to the mask given in Figure 23 with the values given in Table 13 when tested in accordance with Figure 22.

To limit the current that a non-designated terminal can sink from the phantom when connected to PS1 in the restricted mode a non-designated terminal shall conform to the values given below, when tested in accordance with Figure 22:

– TE with connection detector when measured 100 µs after closing the switch shall be less than 3 mW. The TE shall not assume disconnection (transition from any of the states F2 to F8 to state F1 according to Table 3) until the voltage at the interface has remained below 24 V for at least 500 ms.

– TE without connection detector when measured 100 µs after closing the switch shall be less than or equal to 10 µA.

TABLE 13/I.430

PS1 parameters for TE in restricted mode

A	5 µs
Y	(M × 14)mA
C	100 ms
X	Current equivalent to RPCU of TE
M RPCUs drawn by TE	

9.7.1.2 Terminals powered from power source 2

To limit the current that each terminal can sink from the power source when connected to PS2 in normal mode, or when PS2 changes from restricted to normal mode, the terminal shall conform to the mask given in Figure 23 with the values given in Table 14, when tested in accordance with Figure 22.

TABLE 14/I.430

PS2 parameters for TE in normal mode

A	5 µs
Y	(N × 5.5)mA
C	100 ms
X	Current equivalent to NPCU of TE
N NPCUs drawn from PS2 by TE	

To limit the current that a designated terminal can sink from the power source when connected to PS2 in the restricted condition, a designated terminal shall conform to the mask given in Figure 23 with the values given in Table 15 when tested in accordance with Figure 22.

TABLE 15/I.430

PS2 parameters for TE in restricted mode

A	5 µs
Y	(N × 5.5)mA or (M × 21)mA, whichever is lower
C	100 ms
X	Current equivalent to RPCU of TE
N NPCUs M RPCUs drawn from PS2 by TE	

To limit the current that a non-designated terminal can sink from the power source when connected to PS2 in the restricted mode, a non-designated terminal shall conform to the values given below, when tested in accordance with Figure 22.

– when measured 100 μs after closing the switch, the current shall be less than or equal to 10 μA.

9.7.2 Power source switchover time (PS1 or PS2)

When changing from normal mode to restricted mode, or from restricted mode to normal mode, the transition of the voltage between +34 V and –34 V (or vice versa) shall be less than 5 ms. This time is measured with fixed resistive loads, for both normal and restricted mode, connected to the source with diodes where necessary. The values of the resistors shall be chosen so that the load draws designed PCUs in both restricted mode and normal mode when the power source voltage is at its nominal operating value.

9.7.3 Other TE requirements

9.7.3.1 Minimum TE start up current from power source 1

9.7.3.1.1 Restricted mode

A TE powered from PS1 and designed to operate in restricted mode shall be able to reach operational condition

a) when connected to a source of 40 V open-circuit voltage, current-limited at 9 mA;

b) when connected in parallel with a capacitor of 300 μF, and the combination is connected to a source of 40 V open-circuit voltage, current-limited at 11 mA.

NOTE – A TE shall be considered to have reached operational condition when it initiates the transmission of INFO 3 in response to the reception of INFO 2.

9.7.3.1.2 Normal mode

A TE powered from PS1 and designed to operate in normal mode shall be able to reach operational condition when connected in parallel with up to 3 "nominal" TEs (see Note) such that the total PCU rating does not exceed 80 PCUs, and the combination is connected to a source of 40 V open-circuit voltage, current-limited at 200 mA with a surge current capability of 350 mA for 100 ms.

NOTE – A "nominal" TE means a TE with the following characteristics:

– PS1 input capacitance = 100 μF;

– power consumption = 10 NPCU;

– Internal DC-to-DC converter start-up voltage = 24 V.

9.7.3.2 Minimum TE start up current from power source 2

9.7.3.2.1 Restricted mode

A TE powered from PS2 and designed to operate in restricted mode shall be able to reach operational condition when connected to a source of 40 V open-circuit voltage, current-limited at 50 mA.

9.7.3.2.2 Normal mode

A TE powered from PS2 and designed to operate in normal mode shall be able to reach operational condition when connected to a source of 40 V open-circuit voltage, current-limited at 200 mA with a surge current capability of 350 mA for 100 ms.

NOTE – A terminal manufacturer should ensure that a TE designed to operate in normal mode is also able to reach operational condition when connected in parallel with other identical TEs such that the total PCU rating comes close to, but does not exceed, 80 PCUs, and the combination is connected to a source of 40 V open-circuit voltage, current-limited at 200 mA with a surge current capability of 350 mA for 100 ms.

9.7.3.3 Verification

These requirements (for both normal and restricted mode) may be verified by using the test circuit given in I.6.

9.7.3.4 Protection against short term interruptions

A TE shall not lose an ongoing communication when the provision of power in normal mode or restricted mode is interrupted for less than or equal to 5 ms. This requirement shall only apply after power has been continuously provided to the TE for at least 10 seconds.

9.7.3.5 Behaviour at switch-over

A designated TE being in normal mode may change to the restricted mode conditions including power consumption limitation immediately after detection of an interruption of power (in order to protect an ongoing communication by reducing its power consumption).

When the change from normal mode with 32 V to the restricted mode occurs, the designated TE should not lose an established call when the power source for the restricted mode provides an open circuit voltage of 40 V with a limited current of (M × 2.75)mA. The TE shall be able to reach the steady state which allows the power source to leave the current limiting condition.

A designated TE being in restricted mode and detecting transition to normal mode shall not change its power consumption limit from rated RPCU to rated NPCU before 500 ms after detection of the reversed polarity.

NOTE – This refers to a measurement with a 50 ms integration time as noted in 9.1.3, and does not preclude some possible current surge within the mask given in Figure 23.

9.7.3.6 Effective capacitance at the PS1 or PS2 input to the TE

Requirements given in 9.7.3 and 9.7.4 are based on the assumption that the total effective capacitance at the PS1 or PS2 input to the TE is less than 100 μF under all conditions of normal operation, start-up and switch-over between normal and restricted modes, or vice-versa. For TEs drawing less than 10 NPCU in normal mode, capacitance has been assumed to be less than (N × 10)μF.

9.7.3.7 TE behaviour at low input voltage

If the PS1 or PS2 input voltage at a TE is reduced below the specified minimum operating voltage for any reason (for example, a short-circuit or overload on the bus), the TE input current shall not exceed the values given in Table 16.

TABLE 16/I.430

Maximum TE input current at low voltage

PS1, normal mode	(N × 5.5)mA
PS1, restricted mode	(M × 14)mA
PS2, normal mode	(N × 5.5)mA
PS2, restricted mode	(N × 5.5)mA or (M × 21)mA, whichever is lower
N NPCUs M RPCUs drawn by the TE from PS1 or PS2 as applicable	

9.7.4 Other power source requirements

Two alternative power source implementations concerning overload and short-circuit protection have been taken into account, for both normal and restricted mode:

a) sources limiting the output current (fall back characteristic);

b) sources with switch-on/switch-off characteristic.

NOTE – As defined previously, and as used in the following paragraphs, n is the maximum number of terminals to be fed via the interface, of which a maximum of m terminals may be designated. P and Q are, respectively, the rated NPCUs and RPCUs of the source.

9.7.4.1 Power source 1 restricted mode

– *Requirements for type a) sources*

1) The minimum current shall be (Q × 2.75)mA when the output voltage is forced by a resistive test load to 34 V (even if the source is then in overload condition).

2) The power source shall be able to increase the output voltage from 1 V to 34 V with a risetime of less than 1.5 seconds, within 10 seconds after removal of a short-circuit from its output (60 seconds in the case of interface at the S-reference point) or when switching power onto the interface, with a test load of (Q × 25)µF connected to it.

3) At the switchover from normal mode to the restricted mode the PS1 power source shall provide a minimum current of 9 mA when the voltage is reduced to a level below 1 V (overload condition). For conformance test purposes, the current shall be measured with a load resistor applied for at least 1 second.

– *Requirements for both type a) and type b) sources*

(Only applicable to power sources which are not remotely power fed by the LT and which have internal backup capacity, e.g. a backup battery.)

Power source 1 restricted shall be able to provide for at least 100 ms (130 ms for power sources having an output voltage greater than 42 V) an additional current of 50 mA when the constant current drawn from the source was [(Q – 4) × 2.75]mA before this current surge and will be (Q × 2.75)mA after it. The output voltage shall not drop below the minimum value of 34 V during the test.

9.7.4.2 Power source 1 normal mode

– *Requirements for type a) sources*

1) The minimum current shall be (P × 3)mA when the output voltage is forced by a resistive test load to 34 V (even if the source is then in overload condition).

2) The power source shall be able to increase the output voltage from 1 V to 34 V with a risetime of less than 350 ms, within 10 seconds after removal of a short-circuit from its output (60 seconds in the case of interface at the S-reference point), with a test load of (P × 10)µF connected to it.

– *Requirements for both type a) and type b) sources*

1) When switching power onto the interface, power source 1 normal mode shall provide a minimum current of (P × 4.5)mA for at least 100 ms (130 ms for power sources having an output voltage greater than 42 V). This time shall be measured from the instant when the voltage rises above 30 V, and the voltage shall not fall below 30 V during this time period. After the time of 100 (130) ms, the power source shall be able to provide the power corresponding to the number (P) of PCUs to be fed and the power drop on the interface with the output voltage within the specified limits. Test load shall be resistive, and shall be chosen so that the load draws designed PCUs when the PS1 source voltage is at its nominal operating value.

2) Power source 1 normal shall be able to provide for at least 100 (130) ms an additional current of 50 mA when the constant current drawn from the source was [(P – 10) × 3]mA before this current surge and will be (P × 3)mA after it. The output voltage shall not drop below the minimum value of 34 V during the test.

3) For power sources having output voltage greater than 42 V, the power source shall be able to provide rated NPCUs as soon as the voltage reaches 40 V during start-up or recovery from a short circuit. The source shall meet this requirement with a load of (P × 10)µF connected to its output.

9.7.4.3 Power source 2 restricted mode

– *Requirements for type a) sources*

1) The minimum current shall be (Q × 2.75)mA when the output voltage is forced by a resistive test load to 34 V (even if the source is then in overload condition).

2) The power source shall be able to increase the output voltage from 1 V to 34 V with a risetime of less than 1.5 seconds, within 10 seconds after removal of a short-circuit from its output (60 seconds in the case of interface at the S-reference point) or when switching power onto the interface, with a test load of (Q × 25)μF connected to it.

3) At the switchover from normal mode to the restricted mode the PS2 power source shall provide a minimum current of 50 mA when the voltage is reduced to a level below 1V (overload condition). For conformance test purposes, the current shall be measured with a load resistor applied for at least 1 second.

– *Requirements for both type a) and type b) sources*

Power source 2 restricted shall be able to provide for at least 100 ms (130 ms for power sources having an output voltage greater than 42 V) an additional current of 400 mA when the constant current drawn from the source was [(Q – 21) × 2.75]mA before this current surge and will be (Q × 2.75)mA after it. The output voltage shall not drop below the minimum value of 34 V during the test.

9.7.4.4 Power source 2 normal mode

– *Requirements for type a) sources*

1) The minimum current shall be (P × 3)mA when the output voltage is forced by a resistive test load to 34 V (even if the source is then in overload condition).

2) The power source shall be able to increase the output voltage from 1 V to 34 V with a risetime of less than 350 ms, within 10 seconds after removal of a short-circuit from its output (60 seconds in the case of interface at the S-reference point), with a test load of (P × 10)μF connected to it.

– *Requirements for both type a) and type b) sources*

1) When switching power onto the interface, power source 2 normal mode shall provide a minimum current of (P × 4.5)mA for at least 100 ms (130 ms for power sources having an output voltage greater than 42 V). This time shall be measured from the instant when the voltage rises above 30 V, and the voltage shall not fall below 30 V during this time period. After the time of 100 (130) ms, the power source shall be able to provide the power corresponding to the number (P) of PCUs to be fed and the power drop on the interface with the output voltage within the specified limits. Test load shall be resistive, and shall be chosen so that the load draws designed PCUs when the PS2 source voltage is at its nominal operating value.

2) Power source 2 normal shall be able to provide for at least 100 (130) ms an additional current of 400 mA when the constant current drawn from the source was [(P/2) × 3]mA before this current surge and will be (P × 3)mA after it. The output voltage shall not drop below the minimum value of 34 V during the test.

3) For power sources having output voltage greater than 42 V, the power source shall be able to provide rated NPCUs as soon as the voltage reaches 40 V during start-up or recovery from a short circuit. The source shall meet this requirement with a load of (P × 10)μF connected to its output.

9.8 PS1 direct current unbalance

Passive bus configurations create direct current unbalance in the conductors of the transmit and receive pairs. This current unbalance may affect the proper operation of the NT and TE connected to the bus. Two types of effects must be controlled - those due to individual elements and those due to the interconnection of multiple terminals to create a passive bus configuration.

Requirements are specified for the following elements:

– power source;

– interconnecting wiring;

– connector cords;

– power sinks.

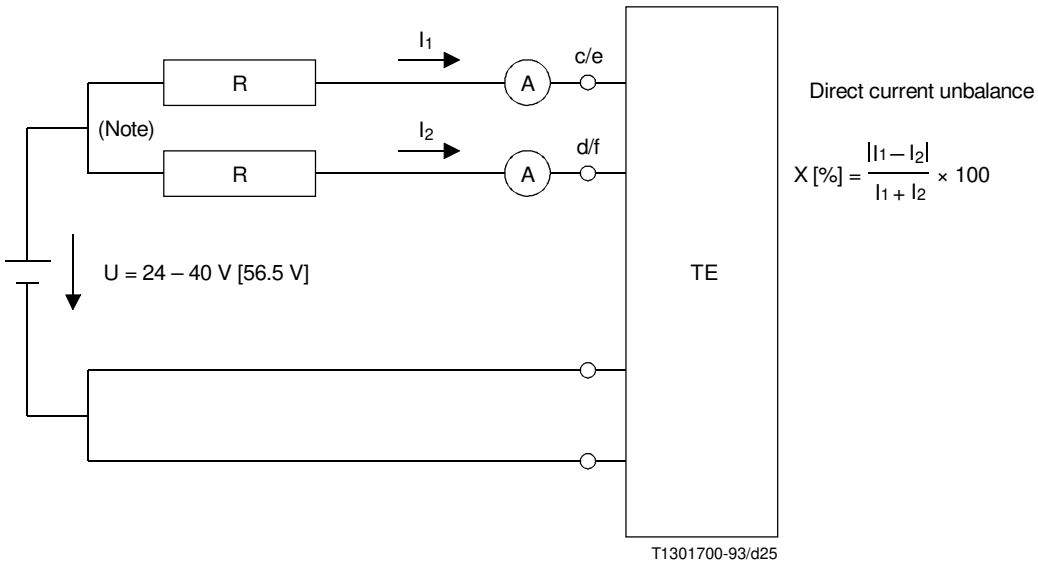
A requirement is also specified to define the effect of the unbalance created by the power sinks of multiple terminals connected to the passive bus. This requirement is intended to assure proper operation under a wide range of applications; however, it does not guarantee operation under a combination of simultaneous worst-case conditions.

9.8.1 TE requirements

9.8.1.1 TE PS1 power sink current balance

The difference in the current in the two sides of each pair (e/f and c/d in Figure 21) of a TE PS1 power sink shall not exceed 3% (of the total current).

Figure 24 illustrates the computation of the direct current unbalance required.



NOTE – The resistors R (2 ohm) represent the TE cord equivalent. They should not be used if the TE has an attached cord.

FIGURE 24/I.430

Circuit for terminal equipment DC unbalance computation

9.8.1.2 Effect of PS1 current unbalance

A TE connected to an installation which includes power source 1 shall meet the electrical characteristics specified in 8.5.1.2, 8.5.3, 8.5.4, 8.5.5.1, and 8.6.1.1 when the PS1 direct current unbalance in each pair is 0.1 mA per PCU (normal or restricted mode).

9.8.2 NT requirements

9.8.2.1 NT power source 1 current balance

The difference in the current in the two conductors of each pair (e/f and c/d in Figure 21) of an NT power source 1 shall not exceed 3% (of the total current) when the NT is operating at its minimum output voltage while providing its rated maximum PCUs (normal or restricted mode), and the terminations associated with each pair are shorted together.

Figure 25 illustrates the computation of the direct current unbalance requirement. Resistors R (2 ohm) simulate a minimum equivalent of the TE cord.

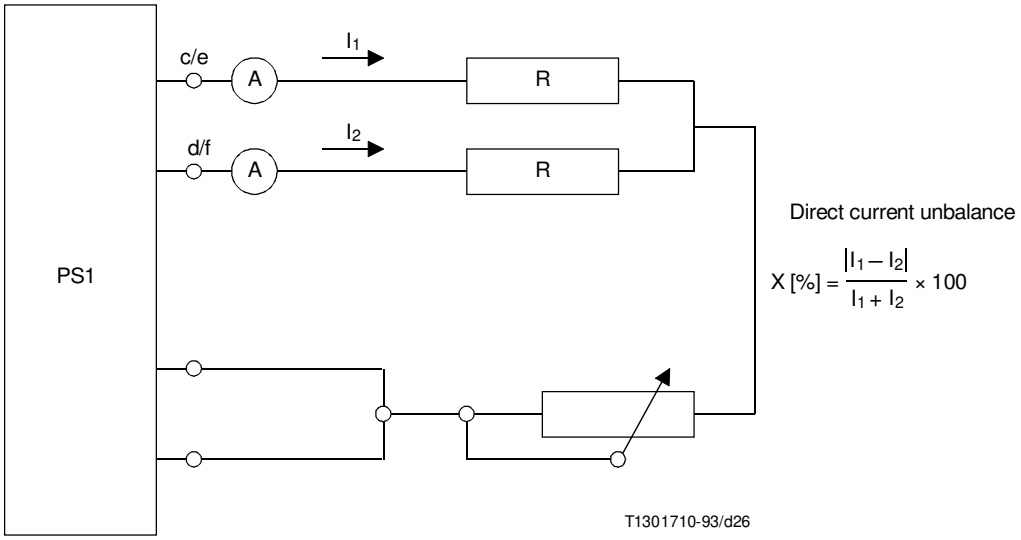


FIGURE 25/I.430

Circuit for power source 1 DC unbalance computation

9.8.2.2 Effect of PS1 current unbalance

An NT, which includes power source 1, shall meet the electrical characteristics specified in 8.5.1.1, 8.5.3, 8.5.4, and 8.6.1.2 when the PS1 direct current unbalance in each pair does not exceed $[(3 \times P)/V_{min}]$mA in normal mode or $[(3 \times Q)/V_{min}]$ in restricted mode. For this calculation, V_{min} is either the minimum designed voltage at the LOAD of the power source or else 30V, whichever is lower.

A circuit configuration to assure proper operation under normal circumstances is shown in Figure I.13.

9.9 Additional requirements for an auxiliary power supply (APS)

Unless otherwise stated, an APS must meet all requirements for PS1 normal mode power sources.

9.9.1 Power available from an APS

The APS power output capability shall be given in terms of NPCUs (see 9.3.1 for definition of NPCU). The NPCU rating shall take account of the power drop on the interface cable, as well as the power required to force the NT1 restricted mode power source to back off, and shall be the power available for the TEs to draw from the interface. The APS shall be designed to have a rating of at least 10 NPCUs.

As an option, an APS may be given different NPCU ratings for different cable configurations, to allow full use of the output power capacity under differing applications (for example, one rating for point-to-point and a different rating for point-to-multipoint).

NOTE – To force the restricted mode power source to back off (relinquish control of the voltage on the phantom), the APS must supply the maximum output current of the restricted mode power source. The restricted mode power source will then be forced to enter a current limiting condition, allowing the polarity and magnitude of the phantom voltage to be controlled by the APS.

9.9.2 APS switch-on time

When the APS switches power onto the interface (e.g. due to the application or restoration of its input power) or when first connected to the bus the voltage across the phantom at the APS output shall rise from 1 V to ≥ 34 V (but shall not exceed 42 V) within 2.5 ms and shall not fall below 34 V for a further period of 2.5 ms.

9.9.3 APS switch-off time

When the APS is no longer able to supply 34 V (for example when it no longer has its required input power) the voltage across the phantom at the APS output shall decay from 34 V to ≤ 1 V within 2.5 ms and shall not rise above 1 V within a further 2.5 ms when tested in isolation from the NT1, with a capacitive load of 100 nF.

In the case where the APS has battery backup, a considerable delay may occur between loss of input power to the APS and APS switch-off. In this case the provision of a "battery low" indication is an acceptable alternative.

9.9.4 APS power consumption when off

The APS shall not consume more than 3 mW from PS1 restricted mode when connected to the bus while APS input power is not available.

9.9.5 Dynamic behaviour of APS

The same requirements as for PS1 normal located inside the NT1 also apply to an APS except that additional capability (equivalent to an additional restricted mode terminal) allows for the support of *n* terminals plus the charge required to force the PS1 restricted mode to back off.

9.10 Additional requirements for NT1 restricted mode source for compatibility with an APS.

The NT1 designed to be compatible with an APS shall not have a PS1 normal mode source. Unless stated otherwise, all PS1 requirements for the restricted mode sources apply.

The APS can also be located inside the same physical equipment as a TE. In this case such a terminal is not to be connected to a network that cannot support the APS (i.e. they do not have "terminal portability").

9.10.1 PS1 restricted mode back-off

The PS1 restricted mode source may have a detector to detect when the normal mode voltage appears on the phantom circuit and switch off the restricted mode source. In this case 9.7.4.1 does not apply.

9.10.2 PS1 restricted mode power-up

When the normal mode voltage at the interface point I_B falls below 5 V, and before it falls to 2 V, the restricted mode source shall drive the phantom voltage into restricted mode (polarity reversal). The risetime from this voltage (+2 V to +5 V) to at least –34 V (but not exceeding –42 V) shall be less than 2.5 ms. The PS1 voltage shall remain within the range of –34 V to –42 V during the following 2.5 ms.

9.10.3 NT1 power consumption from APS normal mode

When the phantom voltage at interface point I_B is within the voltage range 24 V to 42 V the NT1 shall consume ≤ 3 mW.

10 Interface connector contact assignments

The interface connector and the contact assignments are the subject of an ISO standard. Table 17 is reproduced from the International Standard ISO 8877. For the transmit and receive leads, pole numbers 3 through 6, the polarity indicated is for the polarity of the framing pulses. For the power leads, pole numbers 1, 2, 7 and 8, the polarity indicated is for the polarity of the DC voltages under normal power conditions. See Figure 21 for the polarity of the power provided in the phantom mode. In that figure, the leads that are lettered a, b, c, d, e, f, g and h, correspond with pole numbers 1, 2, 3, 6, 5, 4, 7 and 8, respectively.

TABLE 17/I.430

Pole (contact) assignments for 8-pole connections (plugs and jacks)

Pole number	Function		Polarity
	TE	NT	
1	Power source 3 or power sink 3	Power sink 3	+
2	Power source 3 or power sink 3	Power sink 3	–
3	Transmit	Receive	+
4	Receive	Transmit	+
5	Receive	Transmit	–
6	Transmit	Receive	–
7	Power sink 2	Power source 2	–
8	Power sink 2	Power source 2	+

Annex A

Wiring configurations and round trip delay considerations used as a basis for electrical characteristics

(This annex forms an integral part of this Recommendation)

A.1 Introduction

A.1.1 In 4, two major wiring arrangements are identified. These are point-to-point configuration and a point-to-multipoint configuration using a passive bus.

While these configurations may be considered to be the limiting cases for the definition of the interfaces and the design of the associated TE and NT equipments, other significant arrangements should be considered.

A.1.2 The values of overall length, in terms of cable loss and delay assumed for each of the possible arrangements, are indicated below.

A.1.3 Figure 2 is a composite of the individual configurations. These individual configurations are shown in this annex.

A.2 Wiring configurations

A.2.1 Point-to-multipoint

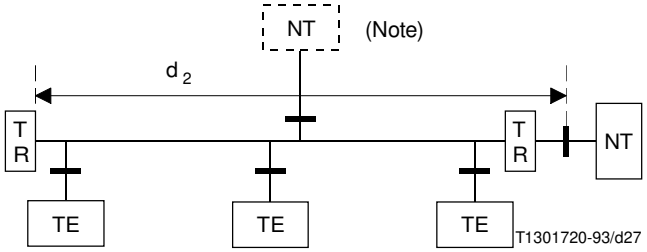
A.2.1.1 The point-to-multipoint wiring configuration identified in 4.2 may be provided by the "short passive bus" or other configurations such as an "extended passive bus".

A.2.1.2 Short passive bus (Figure A.1)

An essential configuration to be considered is a passive bus in which the TE devices may be connected at random points along the full length of the cable. This means that the NT receiver must cater for pulses arriving with different delays from various terminals. For this reason, the length limit for this configuration is a function of the maximum round trip delay and not of the attenuation.

An NT receiver with fixed timing can be used if the round trip delay is between 10 to 14 µs. This relates to a maximum operational distance from the NT in the order of 100-200 metres (d_2 in Figure A.1) [200 m in the case of a high impedance cable (Z_c = 150 ohms) and 100 m in the case of a low impedance cable (Z_c = 75 ohms)]. It should be noted that the TE connections act as stubs on the cable thus reducing the NT receiver margin over that of a point-to-point configuration. A maximum number of 8 TEs with connections of 10 m in length are to be accommodated.

The range of 10 to 14 µs for the round trip delay is composed as follows. The lower value of 10 µs is composed of two bits offset delay (see Figure 3) and the negative phase deviation of –7% (see 8.2.3). In this case the TE is located directly at the NT. The higher value of 14 µs is calculated assuming the TE is located at the far end of a passive bus. This value is composed of the offset delay between frames of two bits (10.4 µs), the round trip delay of the unloaded bus installation (2 µs), the additional delay due to the load of TEs (i.e. 0.7 µs) and the maximum delay of the TE transmitter according to 8.2.3 (15% = 0.8 µs).



TR Terminating resistor

NOTE – In principle, the NT may be located at any point along the passive bus. The electrical characteristics in this Recommendation, however, are based on the NT located at one end. The conditions related to other locations require confirmation.

FIGURE A.1/I.430

Short passive bus

A.2.1.3 Extended passive bus (Figure A.2)

A configuration which may be used at an intermediate distance in the order of 100 to 1000 metres is known as an extended passive bus. This configuration takes advantage of the fact that terminal connection points are restricted to a grouping at the far end of the cable from the NT. This places a restriction on the differential distance between TEs. The differential round trip delay is defined as that between zero-volt crossings of signals from different TEs and is restricted to 2 µs.

This differential round trip delay is composed of a TE differential delay of 22% or 1.15 µs according to 8.2.3, the round trip delay of the unloaded bus installation of 0.5 µs (line length 25 to 50 metres) and an additional delay due to the load of 4 TEs (0.35 µs).

The objective from this extended passive bus configuration is a total length of at least 500 metres (d_4 in Figure A.2) and a differential distance between TE connection points of 25 to 50 metres (d_3 in Figure A.2). (d_3 depends on the characteristics of the cable to be used.) However, an appropriate combination of the total length, the differential distance between TE connection points and the number of TEs connected to the cable may be determined by individual Administrations.

NOTE – Roundtrip delay will normally be in the range of 10 to 26 µs. Where repeaters or amplifiers are utilized, 42 µs is the absolute maximum to ensure proper operation.

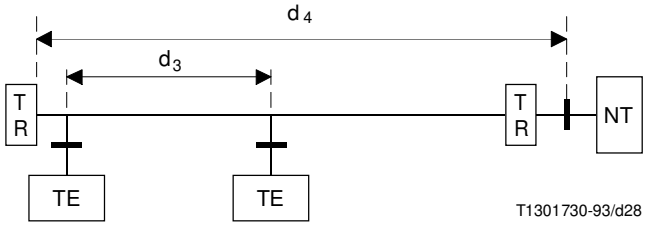


FIGURE A.2/I.430

Extended passive bus

A.2.2 **Point-to-point** (Figure A.3)

This configuration provides for one transmitter/receiver only at each end of the cable (see Figure A.3). It is, therefore, necessary to determine the maximum permissible attenuation between the ends of the cable to establish the transmitter output level and the range of receiver input levels. In addition, it is necessary to establish the maximum round trip delay for any signal which must be returned from one end to the other within a specified time period (limited by D-echo bits).

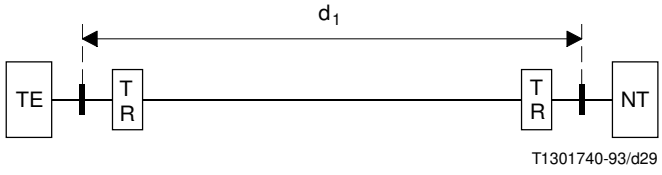


FIGURE A.3/I.430

Point-to-point

A general objective for the operational distance between TE and NT or NT1 and NT2 is 1000 meters (d_1 in Figure A.3). It is agreed to satisfy this general objective with a maximum cable attenuation of 6 dB at 96 kHz. The round trip delay is between 10 to 42 µs.

NOTE – Roundtrip delay will normally be in the range of 10 to 26 µs. Where repeaters or amplifiers are utilized, 42 µs is the absolute maximum to ensure proper operation.

The lower value of 10 µs is derived in the same way as for the passive bus configuration. The upper value is composed of the following elements:

– 2 bits due to frame offset (2 × 5.2 µs = 10.4 µs, see 5.4.2.3.);

– maximum 6 bits delay permitted due to the distance between NT and TE and the required processing time (6 × 5.2 µs = 31.2 µs);

– the fraction (+15%) of a bit period due to phase deviation between TE input and output (see 8.2.3, 0.15 × 5.2 µs = 0.8 µs).

It should be noted that an adaptive timing device at the receiver is required at the NT to meet these limits.

For the NT used for both point-to-point and passive bus configurations (see 8.6.3.2), the tolerable round trip delay in passive bus wiring configurations is reduced to 13 µs due to the extra tolerance required for the adaptive timing. Using this type of wiring configuration, it is also possible to provide point-to-multipoint mode of operation at layer 1.

NOTE – Point-to-multipoint operation can be accommodated using only point-to-point wiring. One suitable arrangement is an NT1 STAR illustrated in Figure A.4. In such an implementation, bit streams from TEs must be buffered to provide for operation of the D-echo channel(s) to provide for contention resolution, but only layer 1 functionality is required. It is also possible to support passive bus wiring configurations on the ports of NT1 STARs. Support of this configuration does not affect the provisions of this Recommendation nor does it affect Recommendations I.441 or I.451.

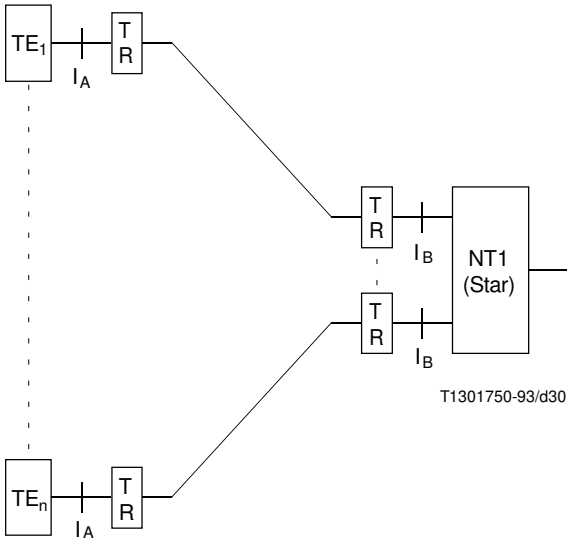


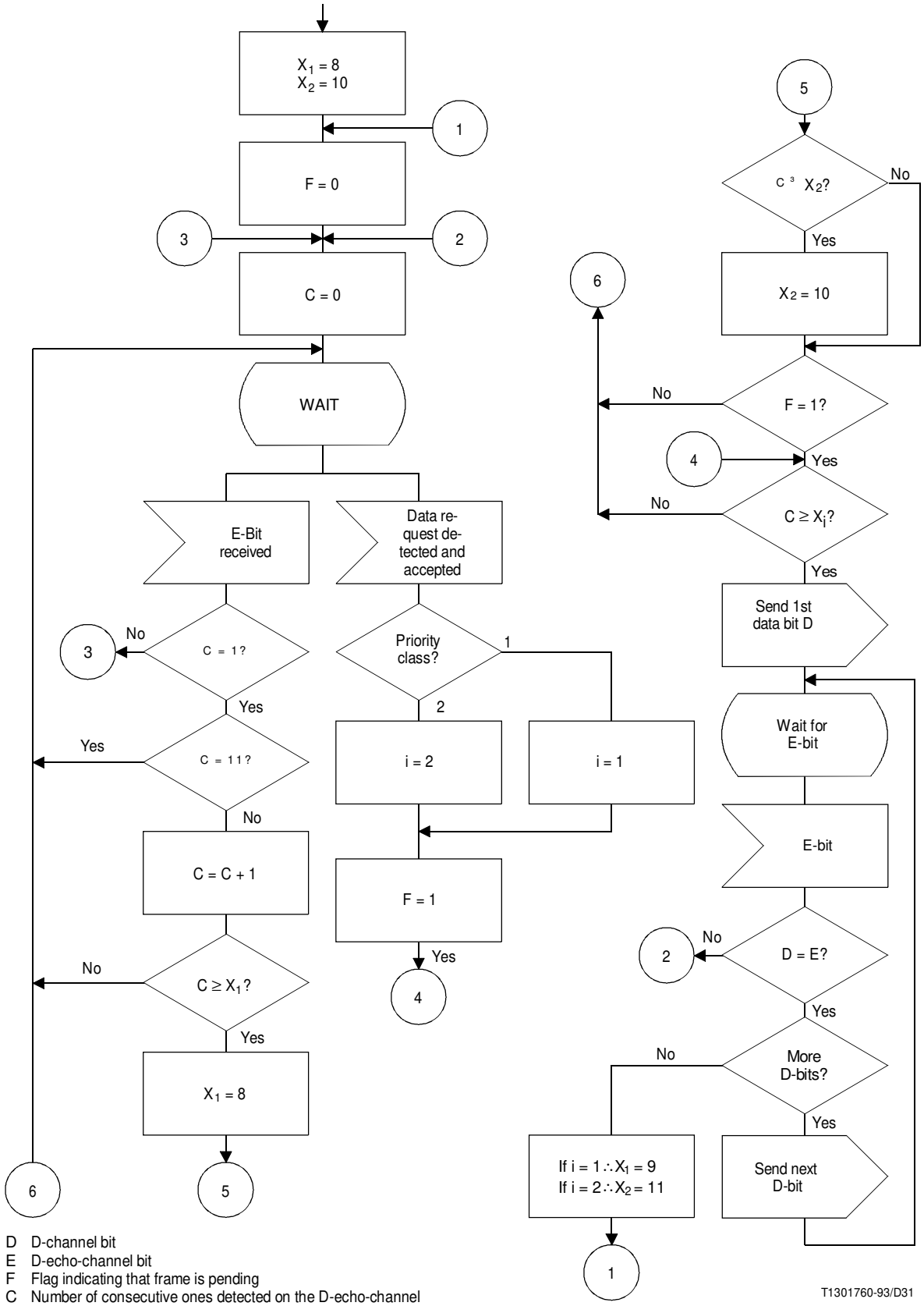
FIGURE A.4/I.430

NT1 Star

Annex B

SDL representation of a possible implementation of the D-channel access

(This annex forms an integral part of this Recommendation)



D D-channel bit
E D-echo-channel bit
F Flag indicating that frame is pending
C Number of consecutive ones detected on the D-echo-channel
X_1 Threshold for priority class 1
X_2 Threshold for priority class 2
i Priority class indicator

Annex C

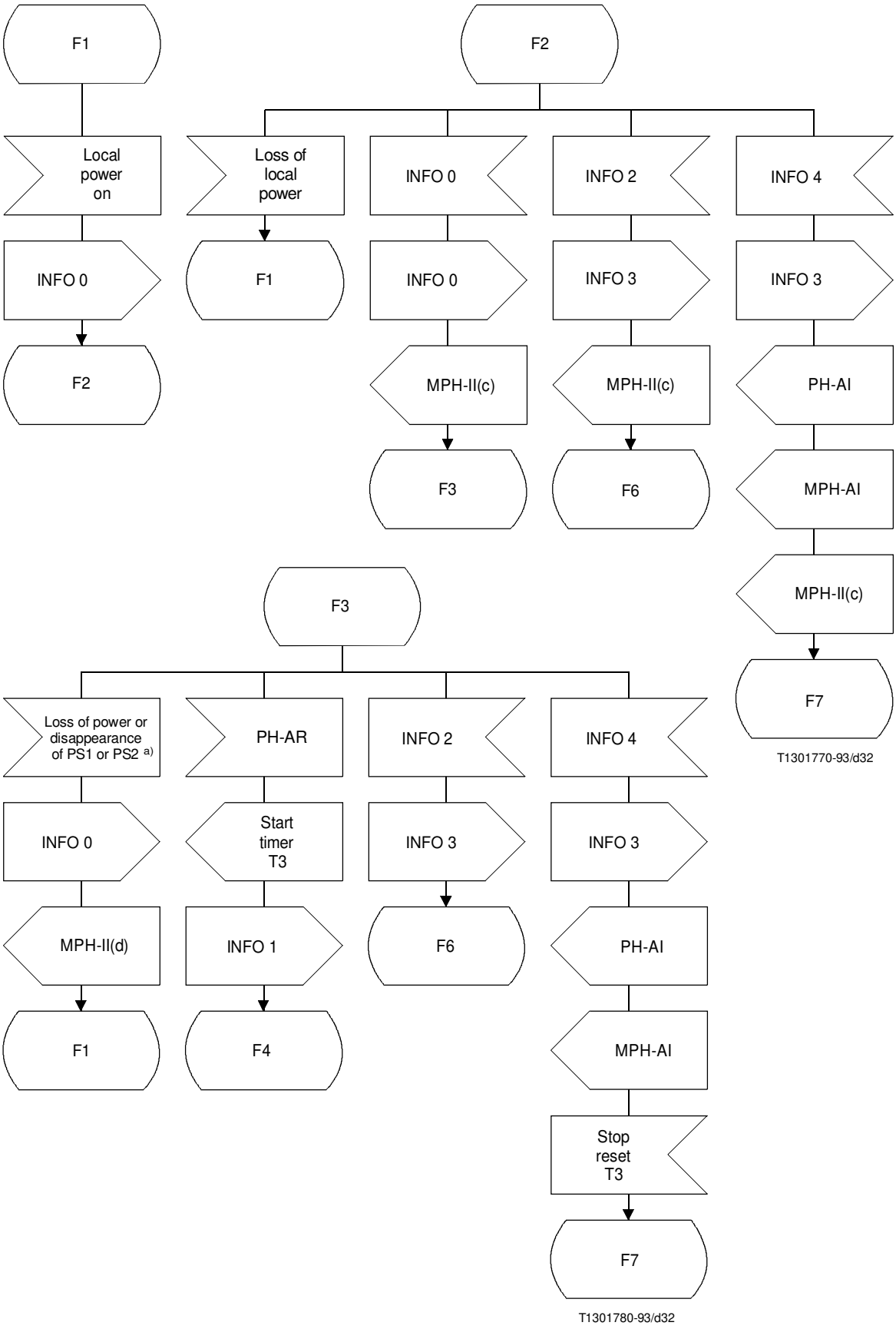
(see Table 5)

(This annex forms an integral part of this Recommendation)

C.1 SDL representation of activation/deactivation procedures for TEs which can detect power source 1 or power source 2 is given in Figure C.1.

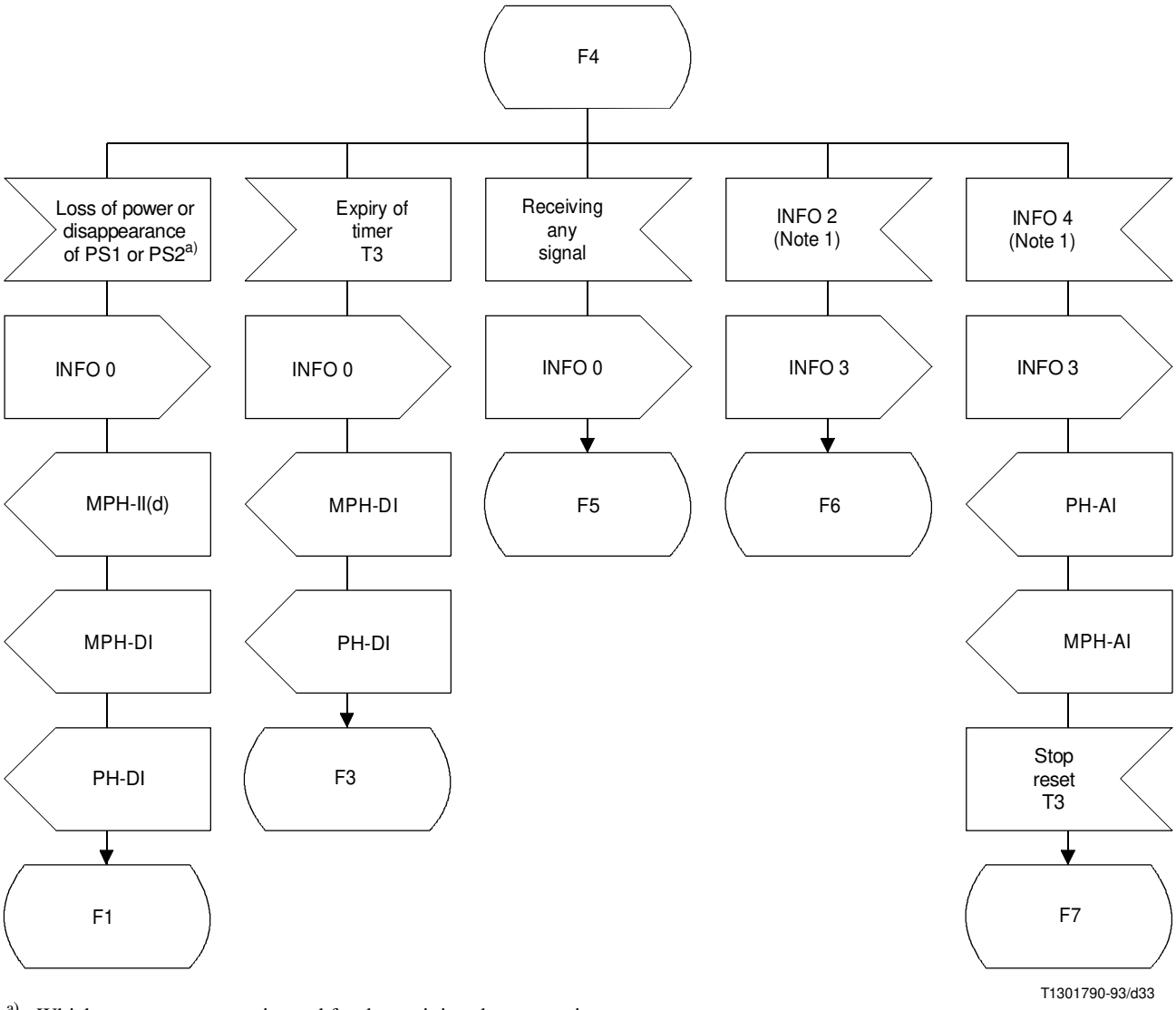
C.2 In 6.2.3 the procedure at the terminal is specified in form of a finite state matrix given in Table 5. This annex provides finite state matrices for two TE types in Tables C.1 and C.2.

C.3 SDL representation of activation/deactivation procedures for NTs (see Table 6) is given in Figure C.2.



a) Whichever power source is used for determining the connection status.

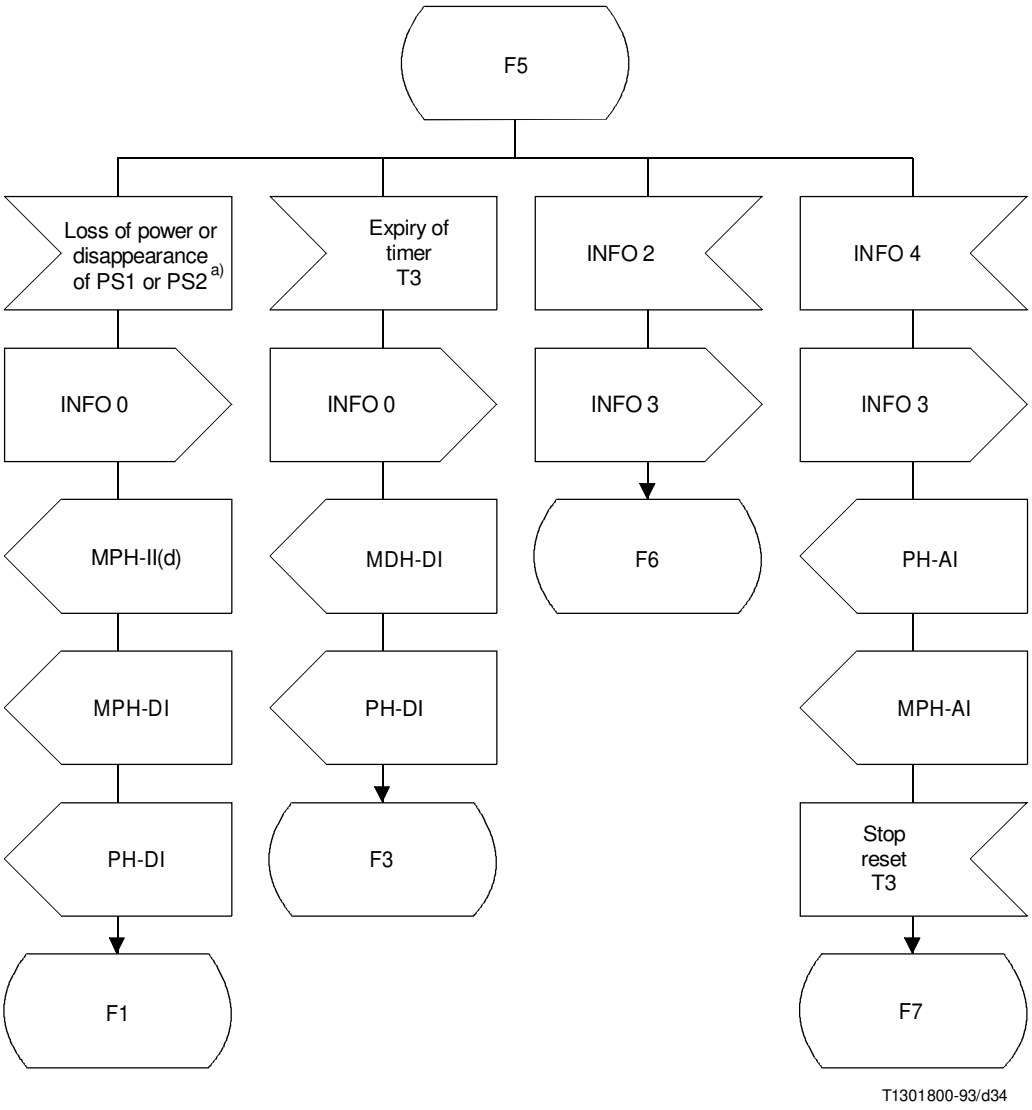
FIGURE C.1/I.430



a) Whichever power source is used for determining the connection status.

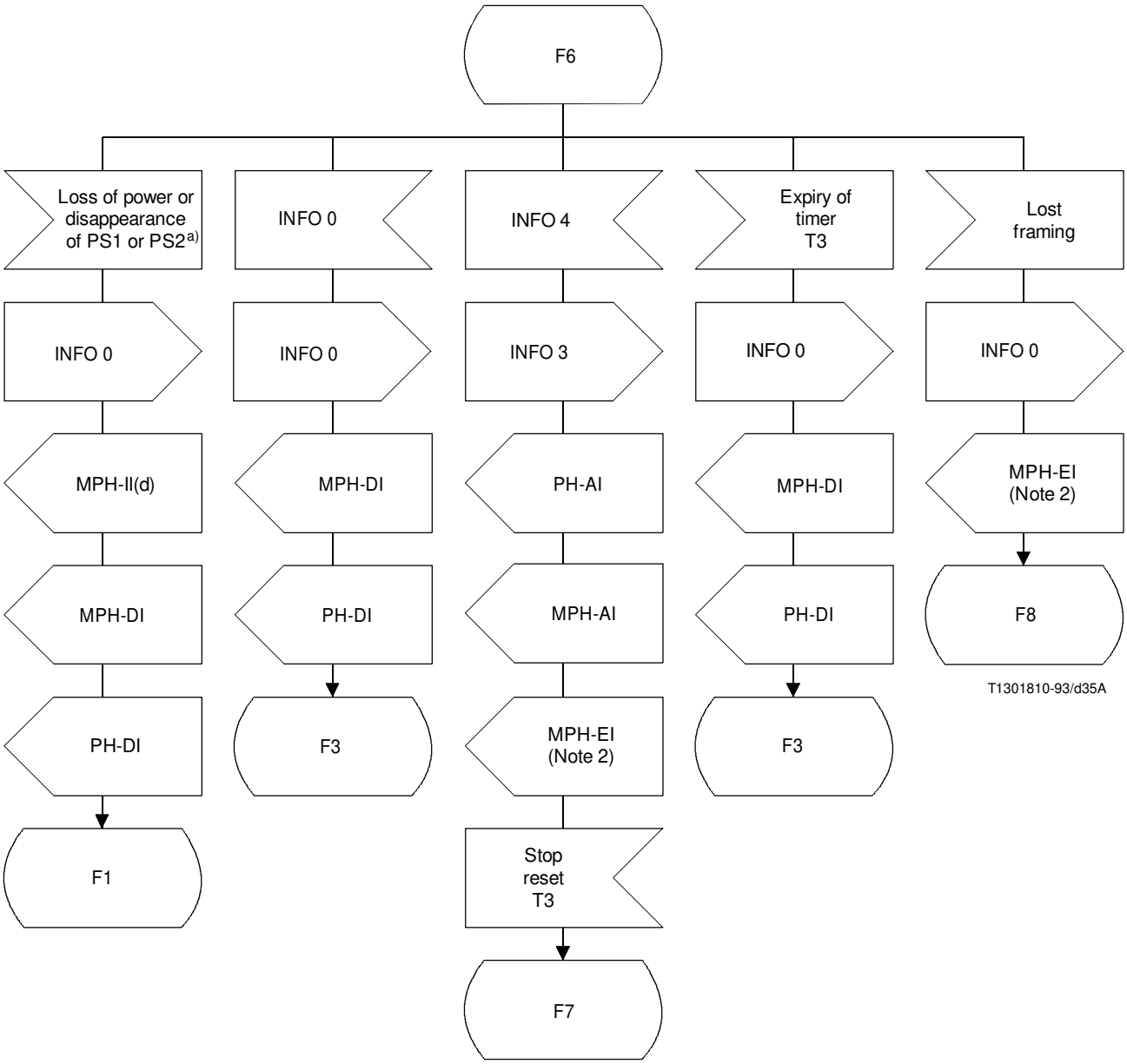
NOTE 1 – If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs must go to F5.

FIGURE C.1/I.430 *(cont.)*



a) Whichever power source is used for determining the connection status.

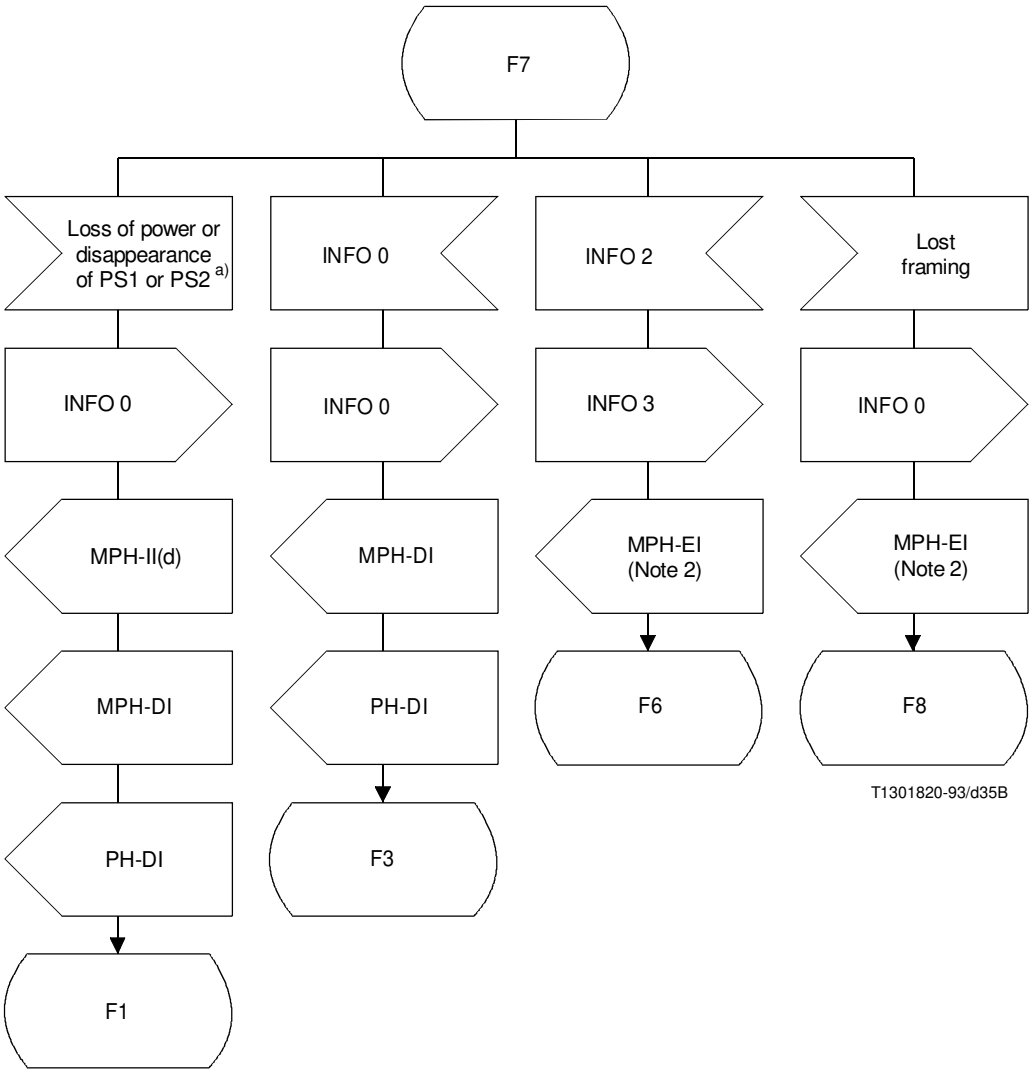
FIGURE C.1/I.430 *(cont.)*



a) Whichever power source is used for determining the connection status.

NOTE 2 – This error indication reports the detection of an error.

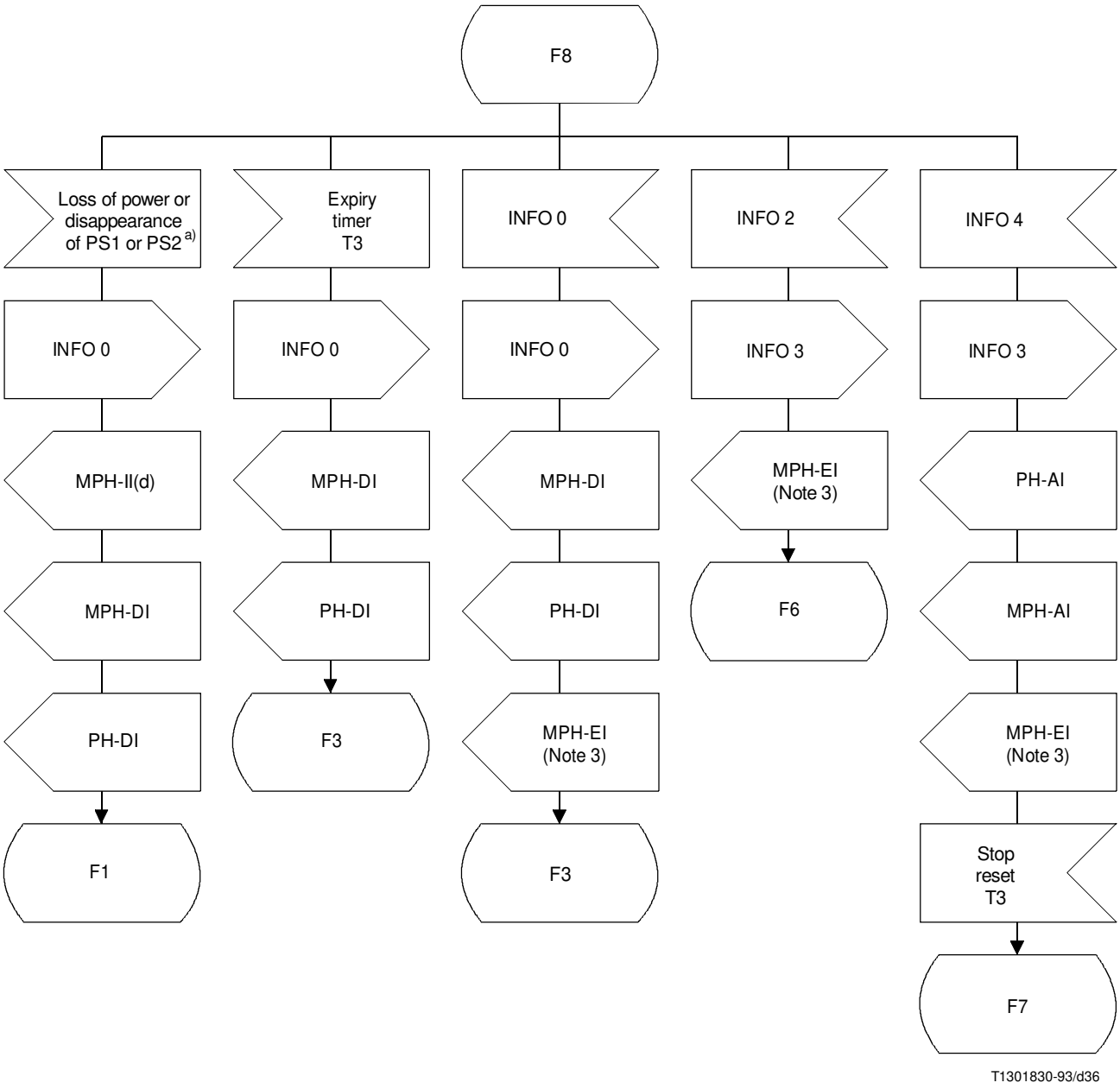
FIGURE C.1/I.430 *(cont.)*



a) Whichever power source is used for determining the connection status.

NOTE 2 – This error indication reports the detection of an error.

FIGURE C.1/I.430 *(cont.)*



PH-AI	Primitive PH-ACTIVATE indication
MPH-AI	Primitive MPH-ACTIVATE indication
MPH-DI	Primitive MPH-DEACTIVATE indication
PH-DI	Primitive PH-Deactivate indication
MPH-EI	Primitive MPH-ERROR indication including a parameter indicating the cause
MPH-II(c)	Primitive MPH-INFORMATION indication (connected)
MPH-II(d)	Primitive MPH-INFORMATION indication (disconnected)
PH	Layer 1 ←→ layer 2
MPH	Layer 1 ←→ management entity

a) Whichever power source is used for determining the connection status.

NOTE 3 – This error indication reports recovery from a previously reported error.

FIGURE C.1/I.430 *(end)*

TABLE C.1/I.430

Activation/deactivation for TEs

TEs Locally powered and unable to detect power source 1 or 2

	State name	Inactive	Sensing	Deactivated	Awaiting signal	Identifying input	Synchronized	Activated	Lostframing
	State number	F1	F2	F3	F4	F5	F6	F7	F8
Event	INFO sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
Loss of local power (Note 2)		/	F1	MPH-II(d); F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1
Local power on (Note 2)		F2	/	/	/	/	/	/	/
Detect power source		Event not applicable to this type of terminal							
Disappearance of power source		Event not applicable to this type of terminal							
PH-Activate request		/	/	ST T3; F4	|	|	–	|	–
Expiry T3		/	/	–	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	–	–
Receiving INFO 0 (Notes 4 and 5)		/	MPH-II(c); F3	–	–	–	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; MPH-EI2, F3
Receiving any signal (Note 1)		/	–	–	F5	–	/	/	–
Receiving INFO 2		/	MPH-II(c); F6	F6	F6 (Note 3)	F6	–	MPH-EI1; F6	MPH-EI2; F6
Receiving INFO 4		–	MPH-II(c), PH-AI, MPH-AI; F7	PH-AI, MPH-AI; S/R T3 F7	PH-AI, MPH-AI; S/R T3 F7 (Note 3)	PH-AI, MPH-AI; S/R T3 F7	PH-AI, MPH-AI, MPH-EI2; S/R T3 F7	–	PH-AI, MPH-AI, MPH-EI2; S/R T3 F7
Lost framing		/	/	/	/	/	MPH-EI1; F8	MPH-EI1; F8	–

NOTES

1 This event reflects the case in which a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.

2 The term *power* could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI values in memory and maintain the capability of receiving and transmitting layer-2 frames associated with the TEI procedures.

3 If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs must go to F5. To assure that a TE will go to state F5 when receiving a signal to which it cannot synchronize, operation of TEs should be verified where the received signal is any bit pattern (containing at least three ZEROs in each frame interval) to which TEs conforming to 6.3.1.2 are not able to synchronize.

4 To avoid disruption of on-going communication caused by spurious effects, a timer may be started when leaving the state F7 or F8 upon reception of INFO 0. The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter state F7 before expiry of this timer. The value of this timer may be in the range of 500 ms to 1000 ms.

5 Two possibilities exist for the reaction in these cases.

Case 1: "–" (No action) – This reaction is appropriate when INFO 2 and INFO 4 are detected to supplement the connection status.

Case 2: MPH-II(d), MPH-DI, PH-DI, F1.1 – This reaction is appropriate when INFO 4 is detected to supplement the connection status.

TABLE C.2/I.430

Activation/deactivation for TEs
TEs locally powered and able to detect power source 1 or 2

State name	Inactive		Sensing	Deactivated	Awaiting signal	Identifying imput	Synchro-nized	Activated	Lostframing
State number	F1.0	F1.1	F2	F3	F4	F5	F6	F7	F8
Event / INFO sent	INFO 0	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
Loss of power (Note 2)	/	F1.0	F1.0	MPH-II(d); F1.0	MPH-II(d), MPH-DI, PH-DI; F1.0	MPH-II(d), MPH-DI, PH-DI; F1.0	MPH-II(d), MPH-DI, PH-DI; F1.0	MPH-II(d), MPH-DI, PH-DI; F1.0	MPH-II(d), MPH-DI, PH-DI; F1.0
Application of power (Note 2)	F1.1	/	/	/	/	/	/	/	/
Detect Power S	/	F2	/	/	/	/	/	/	/
Disappearance of power source	/	/	F1.1	MPH-II(d); F1.1	MPH-II(d); F1.1	MPH-II(d), MPH-DI, PH-DI; F1.1	MPH-II(d), MPH-DI, PH-DI; F1.1	MPH-II(d), MPH-DI, PH-DI; F1.1	MPH-II(d), MPH-DI, PH-DI; F1.1
PH Activate request	/	|	|	ST.T3; F4	|	|	–	|	–
Expiry T3	/	–	–	–	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	–	–
Receiving INFO 0 (Note 4)	/	/	MPH-II(c), F3	–	–	–	MPH-DI, PH-DI; F3	MPH-DI, PH-DI; F3	MPH-DI, PH-DI, MPH-EI2; F3
Receiving any signal (Note 1)	/	/	–	–	F5	–	/	/	–
Receiving INFO 2	/	/	–	F6	F6 (Note 3)	F6	–	MPH-EI1; F6	MPH-EI2; F6
Receiving INFO 4	/	–	MPH-II(c), PH-AI, MPH-AI; F7	PH-AI, MPH-AI; F7	PH-AI, MPH-AI; F7 (Note 3)	PH-AI, MPH-AI; F7	PH-AI, MPH-AI, MPH-EI2; F7	–	PH-AI, MPH-AI, MPH-EI2; F7
Lost framing	/	/	/	/	/	/	MPH-E11; F8	MPH-E11; F8	–

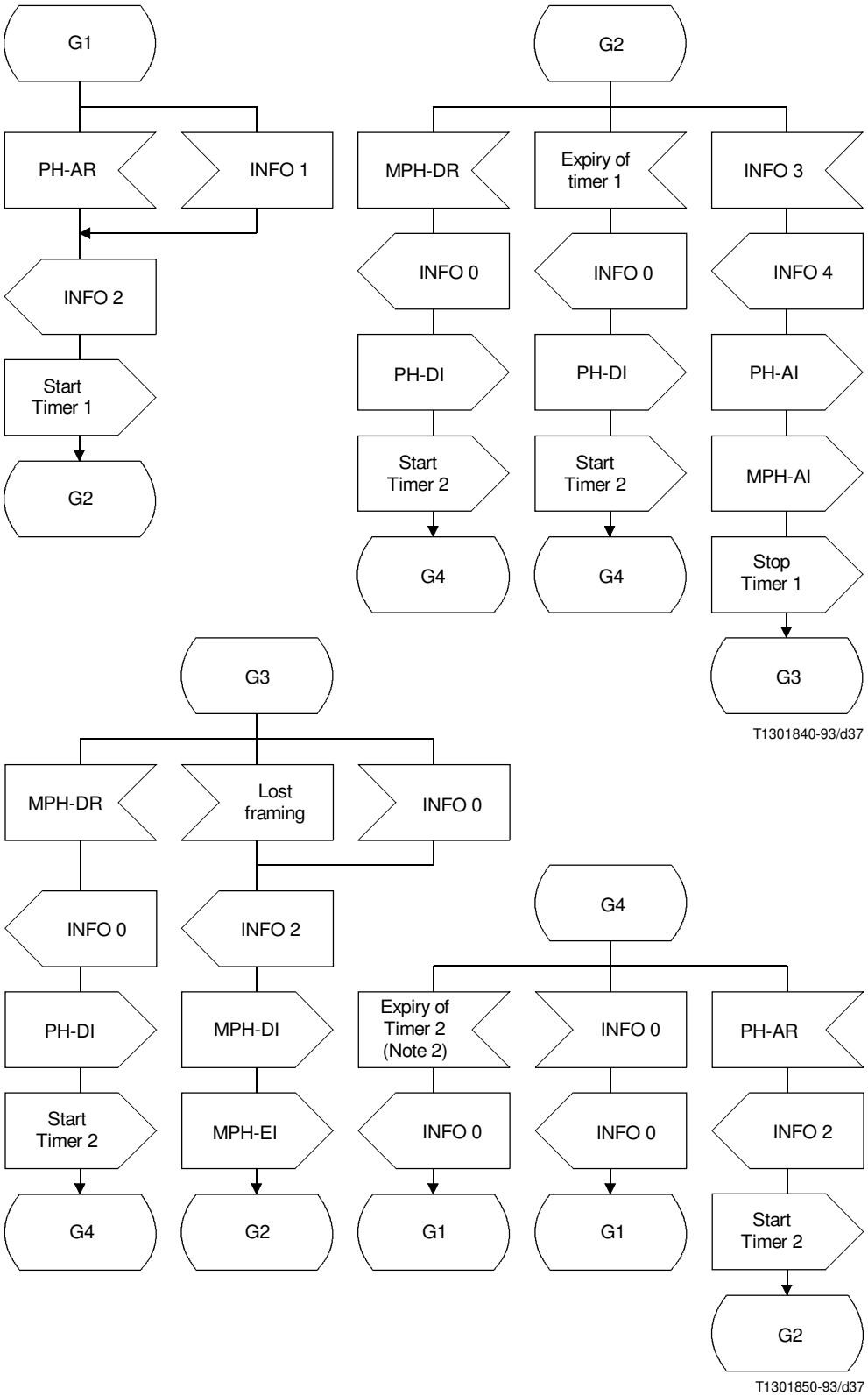
NOTES

1 This event reflects the case in which a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.

2 The term *power* could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI values in memory and maintain the capability of receiving and transmitting layer-2 frames associated with the TEI procedures.

3 If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs must go to F5. To assure that a TE will go to state F5 when receiving a signal to which it cannot synchronize, operation of TEs should be verified where the received signal is any bit pattern (containing at least three binary ZEROs in each frame interval) to which TEs conforming to 6.3.1.2 are not able to synchronize.

4 To avoid disruption of on-going communication caused by spurious effects, a timer may be started when leaving the state F7 or F8 upon reception of INFO 0. The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter state F7 before expiry of this timer. The value of this timer may be in the range of 500 ms to 1000 ms.



NOTES

1 The notifications MPH-DI and MPH-EI need not be transferred to the management entity at the NT.

2 The duration ot Timer 2 is network dependent (25 to 100 ms). This implies that a TE has to recognize INFO 0 and to react on it within 25 ms. If the NT is able to unambiguously recognize INFO 1, then the value of Timer 2 may be 0.

FIGURE C.2/I.430

Annex D

Test configuration

(This annex forms an integral part of this Recommendation)

In 8, waveforms are shown for testing NT and TE equipment. This annex describes configurations, for testing TE equipment, which can be used to generate these waveforms (see Figure D.1). Similar configurations can be used to test NT equipment.

Table D.1 gives the parameters for the artificial lines reproduced in Figure D.1. The artificial lines are used to derive the waveforms. For test configurations ii) and iii), the cable length used corresponds to a signal delay of 1 µs.

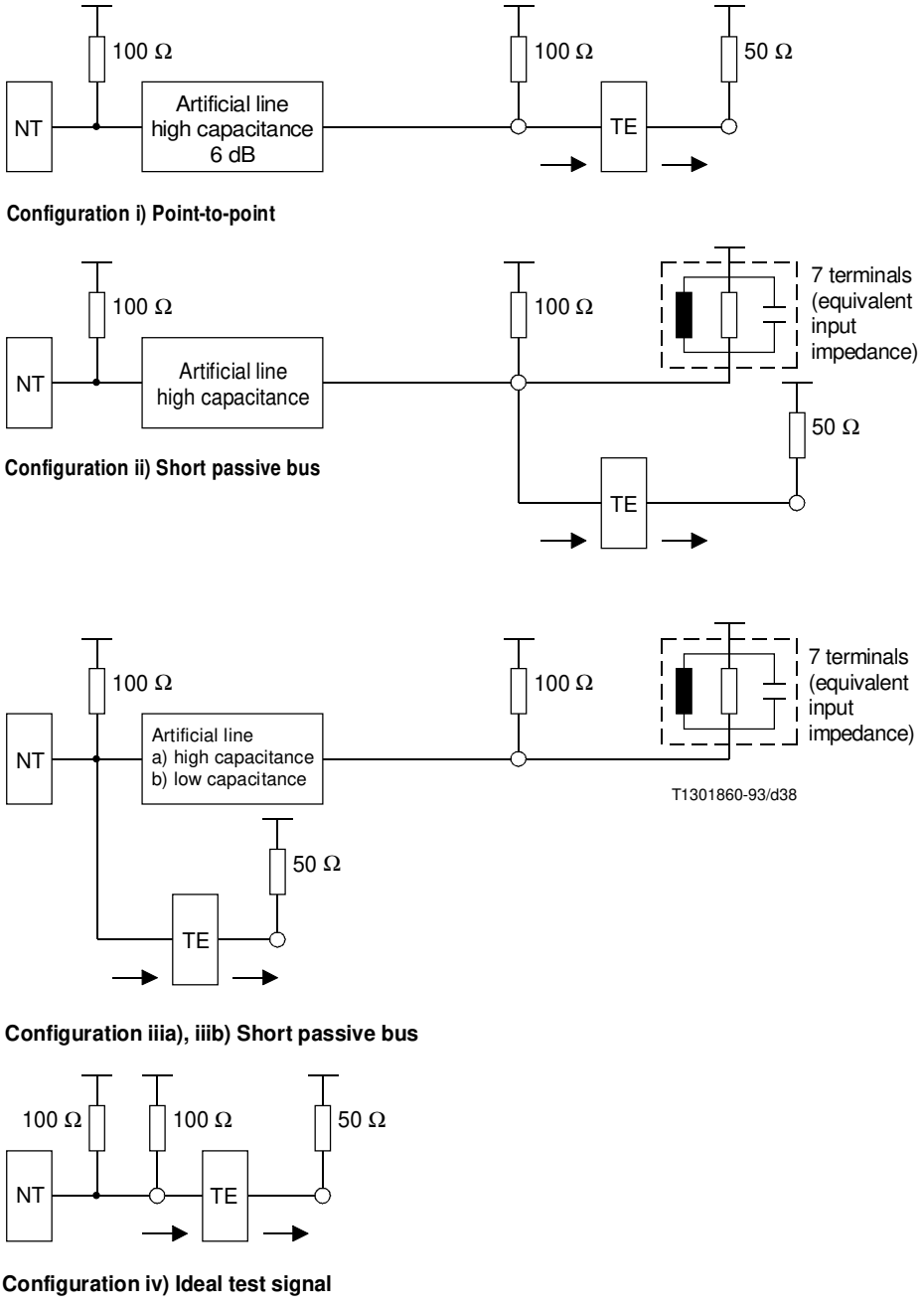


FIGURE D.1/I.430

Test configurations

TABLE D.1/I.430

Parameters for the artificial lines

Parameters	High capacitance cable	Low capacitance cable
R (96 kHz)	160 ohms/km	160 ohms/km
C (1 kHz)	120 nF/km	30 nF/km
Zo (96 kHz)	75 ohms	150 ohms
Wire diameter	0.6 mm	0.6 mm

Appendix I

Testing methods

(This appendix does not form an integral part of this Recommendation)

I.1 Introduction

This appendix provides test configurations and methods to demonstrate compliance with requirements defined in the body of this Recommendation. Other equivalent methods, not described in this appendix, may also be acceptable to demonstrate compliance. The test configurations shown in this appendix are intended to illustrate a conceptual presentation of the test stimulus and not to show a complete circuit for measurement of the characteristics of the unit under test. The requirements are fully specified within the body of the Recommendation, and have precedence over this appendix. The test configurations are intended to cover a reasonable range of permitted conditions.

I.1.1 Basic assumptions for test

As the temperature at which the tests are carried out may affect the results, the effect of temperature shall be taken into account in the testing activity.

TEs using detachable connecting cords and designed for connection with a “standard ISDN basic access cord” shall meet the specified electrical characteristics in both cases as follows:

a) with the specific cord (if any) provided with the TE under test;

b) with a reference cord conforming to the following requirements (see Table I.1)

For a number of tests, information is required about the communication between layer 1 and higher layers to verify all correct behaviour of an implementation. The test specification is based on the fact that such information is available.

TABLE I.1/I.430

Reference cord parameters

Parameter	C	Z	CL	R	D	L
Value	350 pF	> 75 ohms	> 60 dB	3 ohms	< 0.5%	Depends on the other parameters (see Note)
Tolerance	+0/–10%	–	–	+0/–10%	–	

C Capacitance of pairs for transmit and receive functions;

Z Characteristic impedance of pairs used for transmit and receive functions, measured at 96 kHz;

CL Crosstalk loss at 96 kHz between any pair and a pair to be used for transmit or receive functions with terminations of 100 ohms;

R Resistance of individual conductor;

D Difference of the ohmic resistance in each pair used for transmit or receive functions (percentage of the ohmic loop resistance);

L Length of cord.

NOTE – The total length of the cord depends on the parameters shown above. Nevertheless, this length must preferably be equal to 7 m and in any case must be less than 10 m.

I.2 D-channel tests

I.2.1 D-echo channel

To check that the NT, on receipt of a D-channel bit from the TE simulator reflects the binary value in the next available D-echo channel bit position towards the TE, as defined in 6.1.2.

When the TE simulator sends D-bit binary ZERO, returned binary value in the next available D-echo channel bit position towards the TE must be ZERO.

When the TE simulator sends D-bit binary ONE, returned binary value in the next available D-echo channel bit position towards the TE must be ONE.

I.2.2 D-echo channel response

To check that the TE detects collision on the D-channel when transmitting, by means of the D-echo channel, and ceases transmission immediately, and to check that the TE changes priority level correctly within its priority class. As defined in 6.1.4.

Test (a) "mismatch"

Ensure that when the TE receives a binary ONE instead of a binary ZERO (network error) or a binary ZERO instead of a binary ONE (collision), the TE detects the mismatch and ceases transmission immediately, i.e. the next D-bit received from the TE following the application of the stimulus is set to the idle condition (binary ONE). This has to be ensured in each priority class and level which apply to the TE (see Note).

NOTE – The value of subsequent bits is related to priority class and priority level within the class and is covered by test (b) and (c).

The test must be performed with binary ONE and binary ZERO.

Test (b) "priority class"

Ensure that after receipt by the TE of an errored D-echo channel bit, the TE while at the normal priority level receives at least 8 (for priority class 1) or at least 10 (for priority class 2), according to the priority class of the layer 2 frame to be transmitted, contiguous D-echo channel bits set to binary ONE before transmission recommences.

Test (c) "priority level"

Ensure that after successful transmission of a layer 2 frame, the TE:

- does not commence the transmission of a subsequent layer 2 frame until after the receipt of at least 9 (for priority class 1) or at least 11 (for priority class 2), contiguous D-echo channel bits set to binary ONE;

- does change back to normal priority level after the receipt of at least 9 (for priority class 1) or at least 11 (for priority class 2) contiguous D-echo channel bits set to binary ONE if no frame is available to be transmitted.

I.3 Interface procedure tests

I.3.1 Activation/Deactivation procedures

The procedures as defined in 6.2 shall be verified by application of possible state transitions as defined in Tables I.2 and I.3:

TABLE I.2/I.430

Activation/Deactivation tests – NT side

Test number	Current state	Stimulus	Note	Next state	INFO sent	Comment
1	G1	PH-AR	5	G2	I2	Initiate activation and T1
2	G1	T1 expires		G1	I0	No action
3	G1	T2 expires		G1	I0	No action
4	G1	Rx INFO 0	4	G1	I0	No action
5	G1	Rx INFO 1	5	G2	I2	Activation by TE and T1
6	G2	MPH-DR	2	G4	I0	Initiate deactivation and T2
7	G2	T1 expires	2 and 5	G4	I0	Initiate deactivation and T2
8	G2	T2 expires		G2	I2	No action
9	G2	Rx INFO 0	4	G2	I2	No action
10	G2	Rx INFO 1		G2	I2	No action
11	G2	Rx INFO 3	3	G3	I4	Activate and stop T1
12	G3	MPH-DR	2	G4	I0	Initiate deactivation and T2
13	G3	T2 expires		G3	I4	No action
14	G3	Rx INFO 0	1 and 4	G2	I2	Pending deactivation
15	G3	Rx INFO 3		G3	I4	No action
16	G3	Lost framing		G2	I2	Loss of framing signalling
17	G4	PH-AR	5	G2	I2	Initiate activation and T1
18	G4	T1 expires		G4	I0	No action
19	G4	T2 expires	2	G1	I0	Deactivated
20	G4	Rx INFO 0	4	G1	I0	Deactivated
21	G4	Rx INFO 1		G4	I0	No action
22	G4	Rx INFO 3		G4	I0	No action
23	G4	Lost framing		G4	I0	No action

NOTES

1 For testing purposes, INFO 0 is simulated by a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range 2 kHz to 1000 kHz). The NT shall react by transmitting INFO 2 within a time period of 250 µs to 25 ms.

2 If the value of the Timer T2 is 0, a direct transition from state G2 or G3 to G1 is possible (see Note 2 of Table 6).

3 A minimum period of 100 ms can elapse before the sending of INFO 4 or sending of the primitives PH-AI and MPH-AI (see Note 4 of Table 6).

4 INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received.

5 Timer 1 is a supervisory timer which has to take the overall time to activate into account. This time includes the time it takes to activate both the ET-NT and the NT-TE sections of the customer access. ET is the exchange termination.

TABLE I.3/I.430

Activation/Deactivation tests – TE side

Test number	Current state	Stimulus	Note	Next state	INFO sent	Comment
1	F1	Power	1	F2	I0	Detection of power
2	F1	T3 expires	2 and 6	F1	I0	No d'action
3	F2	Loss of power		F1	I0	Return to inactive state
4	F2	Rx INFO 0		F3	I0	Assume deactivated state
5	F2	Rx INFO 2		F6	I3	Synchronized state
6	F2	Rx INFO 4		F7	I3	Activated
7	F2	Rx any signal	3	F2	I0	No action
8	F2	T3 expires	6	F2	I0	No action
9	F3	Loss of power		F1	I0	Return to inactive
10	F3	PH-AR		F4	I1	Initiate activation and T3
11	F3	Rx INFO 0		F3	I0	No action
12	F3	Rx INFO 2		F6	I3	Synchronized state
13	F3	Rx INFO 4		F7	I3	Activated
14	F3	Rx any signal	3	F3	I0	No action
15	F3	T3 expires	2	F3	I0	No action
16	F4	Loss of power		F1	I0	Return to inactive state
17	F4	Rx INFO 0	4	F4	I1	No action
18	F4	Rx INFO 2	7	F6	I3	Synchronized
19	F4	Rx INFO 4	7	F7	I3	Active
20	F4	Rx any signal	3	F5	I0	Detection of signal
21	F4	T3 expires	2	F3	I0	Desactivated
22	F5	Loss of power		F1	I0	Return to inactive
23	F5	Rx INFO 0	4	F5	I0	No action
24	F5	Rx INFO 2		F6	I3	Synchronized
25	F5	Rx INFO 4		F7	I3	Activated
26	F5	Rx any signal	3	F5	I0	No action
27	F5	T3 expires	2	F3	I0	Desactivated
28	F6	Loss of power	8	F1	I0	Return to inactive
29	F6	Lost framing		F8	I0	Loss of framing signals
30	F6	PH-AR		F6	I3	No action
31	F6	Rx INFO 0	4	F3	I0	Desactivated
32	F6	Rx INFO 2		F6	I3	No action
33	F6	Rx INFO 4		F7	I3	Activated
34	F6	T3 expires	2	F6	I3	Synchronized
35	F7	Loss of power	8	F1	I0	Return to inactive
36	F7	Lost framing		F8	I0	Loss of framing
37	F7	Rx INFO 0	4 and 5	F3	I0	Desactivated
38	F7	Rx INFO 2		F6	I3	Synchronized
39	F7	Rx INFO 4		F7	I3	No action
40						
41	F8	Loss of power		F1	I0	Return to inactive
42	F8	PH-AR		F8	I0	No action
43	F8	Rx INFO 0	4 and 5	F3	I0	Desactivated
44	F8	Rx INFO 2		F6	I3	Synchronized
45	F8	Rx INFO 4		F7	I3	Activated
46	F8	Rx any signal	3	F8	I0	No action
47	F8	T3 ex[ires	2	F8	I0	No action

NOTES

1 Because the TE can be powered in different ways, it is recommended to test this item under test (IUT) with the possible power it is able to detect (PS1, PS2, local power).

2 T3 = implementation dependant, not to exceed 30 seconds.

3 "Any signal" is simulated by any bit pattern (containing at least 3 binary ZEROs in each frame interval) on which the IUT conforming to 6.3.1.2 is not able to synchronize.

4 For testing purposes, INFO 0 is simulated by a sinusoidal voltage of 100 mV peak-to-peak (with a frequency in the range 2 kHz to 1000 kHz). The TE shall react by transmitting INFO 0 within a time period of 250 µs to 25 ms.

5 The PH-DI corresponding to the reception of INFO 0 will be delivered to layer 2 only if layer 1 does not re-enter an active state before the expiration of a timer of which the value is in the range of 500 ms to 1 s.

6 Applicable only to TEs which are locally powered and able to detect PS1 or PS2.

7 If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, the TE shall go to F5. The result shall be tested 5 ms after generation of the stimulus.

8 For TEs which are locally powered and able to detect PS1 or PS2, at the event "disappearance of power" in states F6 or F7, no state change must be observed.

I.3.2 Timer for activation/deactivation

Timer defined in 6.2 shall be checked (see Table I.4).

TABLE I.4/I.430

Activation/Deactivation timers

Current state	Stimulus	Notes	INFO sent	Comment
F3	INFO 2		INFO 3	Within 100 ms
F3	INFO 4		INFO 3	Within 100 ms
F4	INFO 2		INFO 3	Within 100 ms; stop INFO 1 within 5 ms
F4	INFO 4		INFO 3	Within 100 ms; stop INFO 1 within 5 ms
F4	any	1	INFO 0	Within 5 ms
F4	INFO 0		INFO 1	After expiry of timer T3 (≤ 30 s) TE shall transmit INFO 0
F6	INFO 0		INFO 0	Within 250 μs to 25 ms
F7	INFO 0		INFO 0	Within 250 μs to 25 ms
F7 or F8	INFO 0 then INFO 4	2	INFO 3	When the duration of INFO 0 is less than 500 ms: no loss of on-going communication When the duration of INFO 0 is more than 1000 ms: loss of on-going communication

NOTES

1 The signal transmitted to the TE is any bit pattern (containing at least three binary ZEROs in each frame interval) to which TEs conforming to 6.3.1.2 are not able to synchronize.

2 This test applies for TEs where layer 3 timer (defined in Recommendation Q.931) is not implemented.

I.4 TE jitter characteristics

I.4.1 TE jitter measurement characteristics

TE jitter requirements defined in 8.2.2.

State: F7

Test configuration to be as shown in Figure I.1.

Stimulus and test results as defined in 8.2.2.

I.4.2 TE output phase offset

State: F7

Test configuration: as given in Figure I.2.

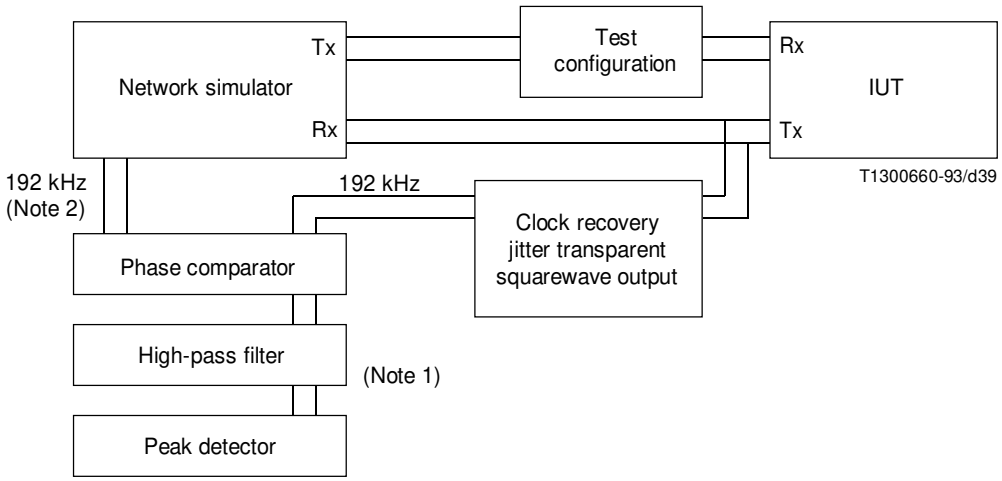
Stimulus and results: as defined in 8.2.3.

I.5 Pulse shape and amplitude

I.5.1 Pulse shape

Pulse shape and amplitude of isolated transmitted pulses (no adjacent pulses).

Both positive and negative pulses shall fit the mask of Figure I.3 with a nominal amplitude of 750 mV zero to peak.



NOTES

1 For measurement purposes, an additional low-pass filter with a cut-off frequency higher than 96 kHz can be added.

2 The clock provided by the network simulator must be synchronous with the signal received by the item under test.

FIGURE I.1/I.430

TE jitter measurement

I.5.2 Pulse unbalance test

Refer to 8.5.4.

A TE under test shall be terminated in 50 ohms; an NT under test shall be terminated in either 50 ohms or 100 ohms depending on whether or not it contains an internal terminating resistor. A frame is generated containing any bit pattern which provides at least two binary ONEs prior to the measured positive or negative pulse (for example, 11011011). If the bit pattern 11011011 is used, the pulses in bit positions 3 and 6 are to be measured. The integration interval begins 2.6 µs before the rising edge and extends to 7.8 µs after the rising edge. The relative difference between the pulses is computed using the following formula:

$$[\text{Area (positive)} - \text{Area (negative)}] \,/\, \{[\text{Area (positive)} + \text{Area (negative)}]/2\}$$

The relative difference must be less than 5%.

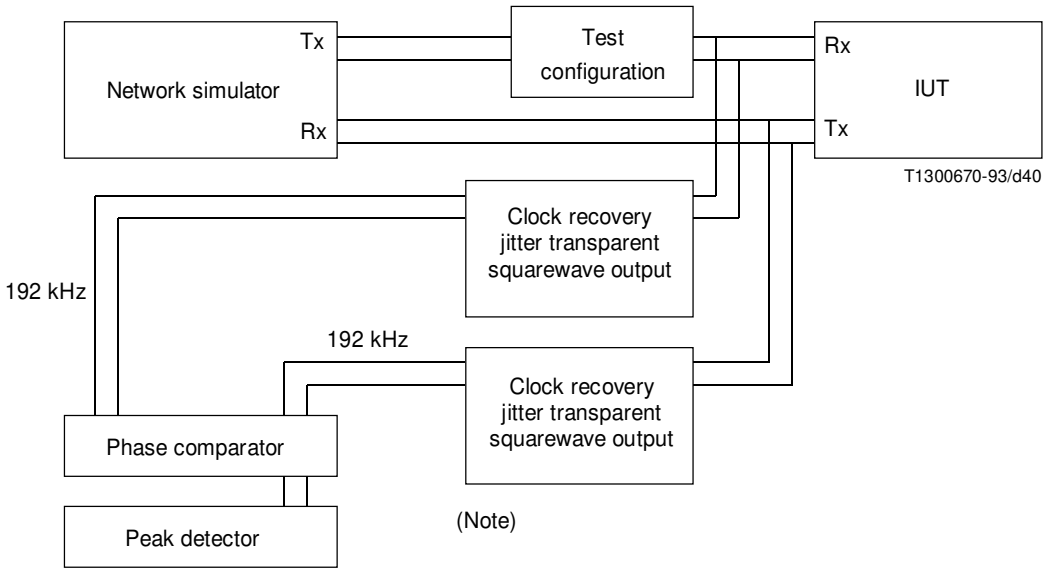
I.6 Terminal power feeding dynamic requirements

I.6.1 Test of TE start-up

Refer to 9.7.3.1.

NOTE – This test applies only for terminals powered from PS1.

A TE shall be able to reach operational condition (i.e. transmission of INFO 3 in response to receipt of INFO 2) when connected to the test circuit given in Figure I.3 with the parameters given in Table I.5 for a TE designed to operate in normal mode, and the parameters given in Table I.6 for a TE designed to operate in restricted mode.



NOTE – For measurement purposes, an additional low-pass filter with a cut-off frequency higher than 96 kHz can be added.

FIGURE I.2/I.430

TE phase offset measurement

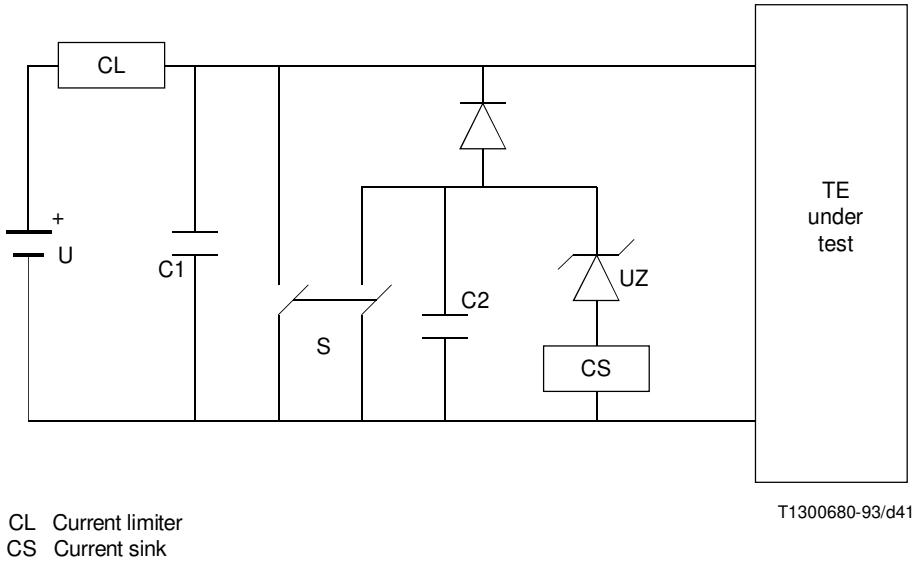


FIGURE I.3/I.430

Test circuit for TE start-up

Before starting the test capacitors C1 and C2 must be discharged by closing switch S. Current sink CS is to be adjusted according to Table I.5 or Table I.6. Then open the switch S for the test. For normal mode the test shall be performed with C1 = 0 µF and C1 = 300 µF.

TABLE I.5/I.430

Parameters for TE in normal mode

U = 40 V	CL = 350 mA	C2 = 2200 µF	C1 = 0 µF
UZ = 24 V	CS = (270 – 1.5 × N) mA		C1 = 300 µF

TABLE I.6/I.430

Parameters for TE in restricted mode

Test a	CL = 9 mA	C1 = 0 µF	C2 = 0 µF CS = 0 mA
Test b	CL = 11 mA	C1 = 300 µF	U = 40 V

In the presence of other equipment connected to the bus, a TE is expected to start upon initial connection, when the NT is connected to the bus, and after the NT recovers from a short circuit. The test configuration shown in Figure I.3 models the installation parameters for a TE. The NT is represented by the voltage source, the CL, and C1. The bridged terminals, approximately three, are represented by the two diodes, the CS, and C2. This circuit is a compromise intended to reflect the complex interactions described in Appendix II.

I.6.2 Current transient

Refer to 9.4.

The maximum allowable rate of change of current drawn by a TE from PS1 is 5 mA/µs, measured from 10% to 90% of any current transients. It should be measured using an oscilloscope with a current probe to sense the PS1 current, and the TE should be controlled in such a way that all possible internal states are exercised. The condition or change of conditions which results in the greatest current transient should be used for the measurement. In addition, the TE should be tested in the condition which results in the highest steady current consumption, to verify that current spikes due to the TE internal DC-to-DC converter do not exceed the specified limit. The test should be carried out at both maximum and minimum TE input voltage.

To avoid measurement problems during this test, the power source used for PS1 should have very low output ripple voltage. Also, TE input current transients with an amplitude less than 1.5 mA may be ignored for this test.

I.6.3 Current/Time limitations for TEs

Refer to 9.7.1.

For the various tests of TE input current under transient conditions specified in 9.7.1, the TE should be connected as given in Figure 22 and the input current (PS1 or PS2 as appropriate) should be measured using an oscilloscope with either a current probe to measure the current directly, or else a voltage probe connected across the resistor R in Figure 22. (A current probe is preferred, since it avoids possible ground loop and noise pickup problems.) In each case, the TE should conform to the appropriate current/time mask given in the body of the Recommendation.

NOTES

1 The mask given in Figure 23 specifies current after the time of 100 ms indirectly, in terms of TE input voltage and PCU rating. Allowance should be made for any voltage drop in the test equipment when calculating the allowable current.

2 After this 100 ms period, a TE is allowed to take short-term surges in current above the calculated value provided that it does not exceed its PCU rating when the current is integrated over a 50 ms period, and provided that it does not exceed the maximum rate of change of input current given in 9.4.

I.6.4 Protection against short-term interruptions

Refer to 9.7.3.4.

The TE should be set up using PS1 or PS2 as appropriate, and a communication established. After power has been present for at least 10 seconds, power should be interrupted for a period of 5 ms and the communication must not be lost. This test should be carried out at the lowest specified operating voltage at the TE, and with all TE functions activated so that it draws maximum power.

I.6.5 TE Behaviour at switchover

Refer to 9.7.3.5.

Before the switchover the input voltage to the designated TE should be 32 V. After switchover to restricted mode, the input voltage to the TE should be –40 V, but fed through a current limiter of the value given in 9.7.3.5. The current limiter must be directly between the source and the TE, with no significant capacitance at the output of the current limiter (refer to Figure I.4). During the switchover, the input voltage to the TE should drop to zero for a period of 5 ms to simulate the maximum allowable switchover time of the PS1 or PS2 power source.

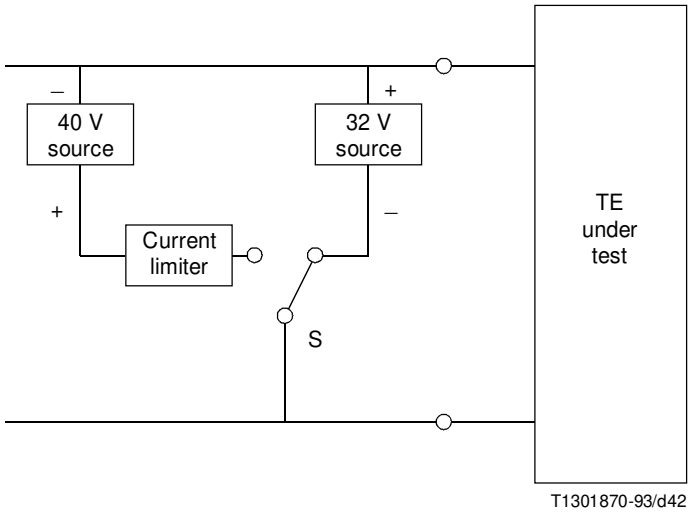


FIGURE I.4/I.430

TEST circuit for TE switchover

The TE should be able to withstand this switchover test without losing an established call, and after the transition, the TE should reach a steady-state condition in which it draws less current than the current limiter value. This may be verified by using an oscilloscope and current probe to monitor the TE input current.

I.6.6 Behaviour at low input voltage

Refer to 9.7.3.7.

The TE should be set up in normal operating mode, with all TE functions activated so that it draws maximum power. Slowly reduce the input voltage to zero, while monitoring the TE input current. The current will initially rise as the voltage is lowered, but will reach a maximum and then start to fall as the input voltage is further reduced. (TE functionality will be lost during this test.) Verify that the maximum current does not exceed the values given in Table 16.

I.7 Power source dynamic requirements

Throughout this clause, P is the rating of the power source PS1/PS2 in normal mode, and Q is the rating of the power source PS1/PS2 in restricted mode. Before carrying out tests of power source dynamic behaviour (see 7.2 to 7.4), the type of power source must first be determined as given in 7.1.

I.7.1 Power source type

Refer to 9.7.4.

Verify whether the power source is type a) or type b), by overloading the power source and observing its behaviour. If the source continues to supply current, it is type a); if it initially switches off (and repeatedly attempts to restart until the overload is removed), it is type b).

I.7.2 Restricted mode requirements for type a) sources only

Refer to 9.7.4.1 and 9.7.4.3.

i) *Output current at 1 V*

Apply a resistive test load to the PS1 or PS2 output (connect through a low-voltage-drop diode) and increase the load until the voltage at the source output is forced to a value of 1 V or less. Apply the mains power input to the power source so that it switches over to normal mode. Disconnect the mains power and monitor the power source output current for at least 1 second after it switches back to restricted mode. It must be at least 9 mA for PS1 or 50 mA for PS2.

ii) *Output current at 34 V*

Apply a resistive test load to the restricted mode source (PS1 or PS2) and monitor the source output voltage. Increase the load until the voltage drops to 34 V, and verify that the source output current is at least $(Q \times 2.75)$mA.

iii) *Rise-time*

Connect the restricted mode source (PS1 or PS2) to a capacitive load of $(Q \times 25)\mu$F, and with a short-circuit across its output. Remove the short-circuit and measure the rise-time of the voltage across the load capacitor to confirm that it meets the requirements given. The time between removing the short-circuit and reaching 34 V must be less than 10 seconds (60 seconds in the case of interface at the S-reference point), and rise-time measured between 1 V and 34 V must be less than 1.5 seconds.

I.7.3 Normal mode requirements for type a) sources only

Refer to 9.7.4.2 and 9.7.4.4.

i) *Output current at 34 V*

Apply a resistive test load to the normal mode source (PS1 or PS2) and monitor the source output voltage. Increase the load until the voltage drops to 34 V, and verify that the source output current is at least $(P \times 3)$mA.

ii) *Rise-time*

Connect the normal mode source (PS1 or PS2) to a capacitive load of value $(P \times 10)\mu$F, and with a short-circuit across its output. Remove the short-circuit and measure the rise-time of the voltage across the load capacitor to confirm that it meets the requirements given. The time between removing the short-circuit and reaching 34 V must be less than 10 seconds (60 seconds in the case of interface at the S-reference point), and rise-time measured between 1 V and 34 V must be less than 350 ms.

I.7.4 Restricted mode requirements for both type a) and type b) sources

i) *PS1 source TE connection surge*

Connect the power source to the loads as shown in Figure I.5. Set up the load L1 so that the source output current is [(Q – 4) × 2.75]mA. Wait at least 10 seconds to ensure conditions are stabilized, and then switch in an additional load L2 with the current/time characteristic shown in Figure I.6, with current values as given in Table I.7. The source output voltage must not drop below 34 V during this test.

ii) *PS2 source TE connection surge*

Connect the power source to the loads as shown in Figure I.7. Set up the load L1 so that the source output current is [(Q – 21) × 2.75]mA. Wait at least 10 seconds to ensure conditions are stabilized, and then switch in an additional load L2 with the characteristic shown in Figure I.6, with current values as given in Table I.8. The source output voltage must not drop below 34 V during this test.

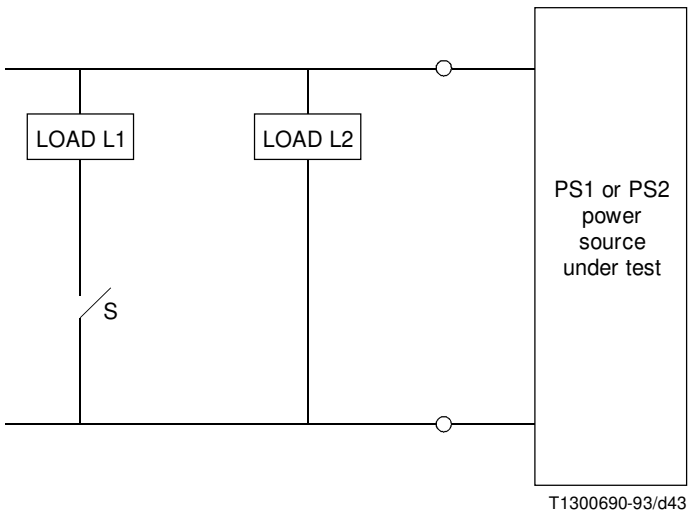


FIGURE I.5/I.430

Power source surge capability test

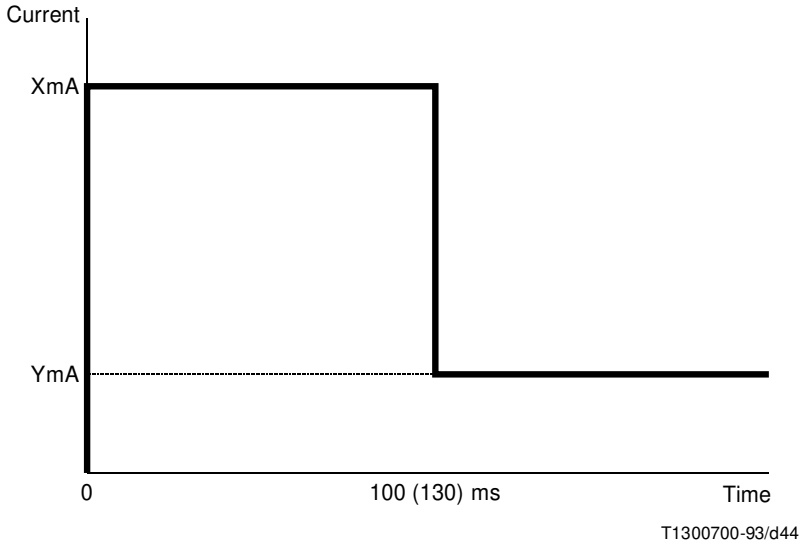


FIGURE I.6/I.430

Load L2 current VS time

TABLE I.7/I.430

Parameters for restricted mode TE connection surge (PS1)

X	61 mA
Y	11 mA

TABLE I.8/I.430

Parameters for restricted mode TE connection surge (PS2)

X	460 mA
Y	60 mA

I.7.5 Normal mode requirements for both type a) and type b) sources

i) *Start-up surge*

Connect the normal mode power source (PS1 or PS2) to the loads as indicated in Figure I.7. When the output voltage is below 30 V, the switch S connects the power source output to the current sink. When the voltage detector detects 30 V at the power source output, it starts a timer. After expiry of the timer, the switch operates to connect the power source output to the static load. The value of the timer is 100 ms (130 ms if the power source output is greater than 42 V).

Set up the static load so that the source is supplying current equivalent to its rated PCUs at its measured output voltage. Set the current sink value to (P × 4.5)mA. Switch off the power at the input to the source, wait 10 seconds and then switch back on. After the output voltage has reached 30 V, it must not drop below 30 V for the test period of 100(130) ms.

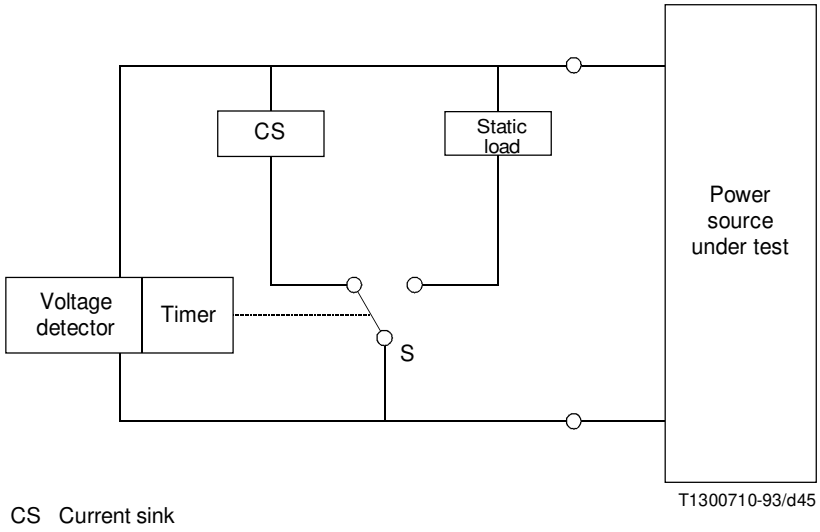


FIGURE I.7/I.430

Test circuit for normal mode start-up surge

ii) *TE connection surge (PS1)*

Connect the power source to the loads as shown in Figure I.5. Set up the load L1 so that the source output current is [(P – 10) × 3]mA. Wait at least 10 seconds to ensure conditions are stabilized, and then switch in an additional load L2 with the characteristic shown in Figure I.6, with current values as given in Table I.9. The source output voltage must not drop below 34 V during this test.

TABLE I.9/I.430

Parameters for normal mode TE connection surge (PS1)

X	80 mA
Y	30 mA

iii) *TE connection surge (PS2)*

Connect the power source to the loads as shown in Figure I.5. Set up the load L1 so that the source output current is [(P/2) × 3]mA. Wait at least 10 seconds to ensure conditions are stabilized, and then switch in an additional load L2 with the characteristic shown in Figure I.6, with current values as given in Table I.10. The source output voltage must not drop below 34 V during this test.

TABLE I.10/I.430

Parameters for normal mode TE connection surge (PS2)

X	[(P/2) × 3] + 400 mA
Y	(P/2) × 3 mA

iv) *Output at 40 V (only for sources having output voltage greater than 42 V)*

Connect the source (PS1 or PS2) as indicated in Figure I.8. The voltage detector is arranged to connect the power sink to the power source when the voltage reaches 34 V. Switch on the power source and monitor the output voltage as it rises to reach the steady-state condition. Verify that once the power source output voltage reaches 40 V, it is capable of providing its rated PCUs, i.e. its output voltage does not drop below 40 V before reaching the steady-state.

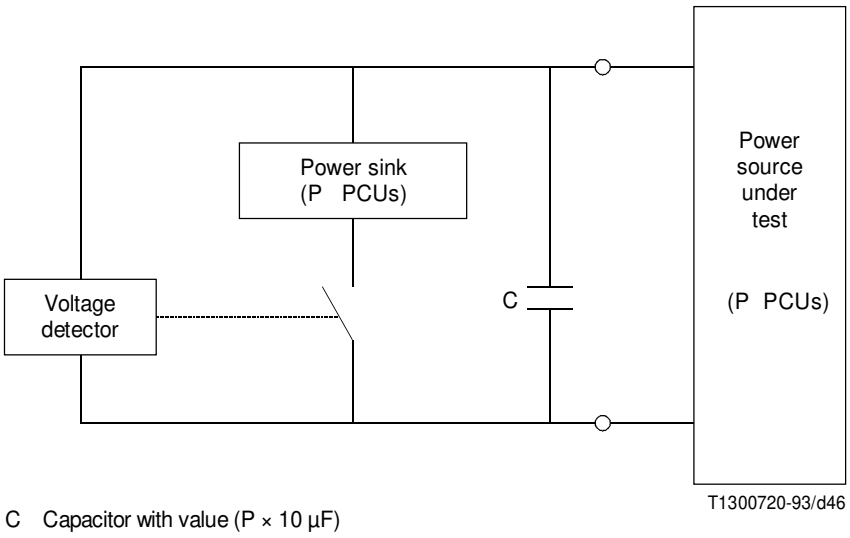


FIGURE I.8/I.430

Start-up test (sources with output voltage greater than 42 V)

I.7.6 Power source switchover

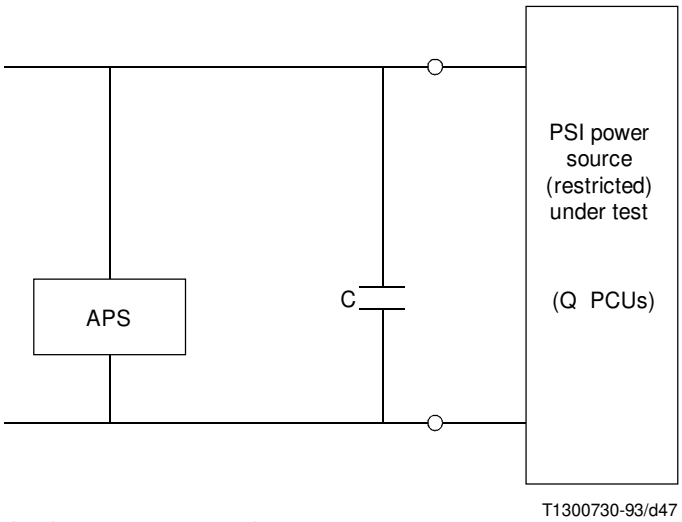
Refer to 9.7.2.

Connect the power source (PS1 or PS2) to fixed resistive loads through diodes so that the total power consumed by the normal and restricted mode loads (including the associated diode) at the power source steady-state output voltage is equal to the corresponding power source PCU rating. Monitor the output voltage as the power source mains input is alternately applied and removed, using an oscilloscope. Verify that the transition time between 34 V in one polarity and 34 V in the opposite polarity is less than 5 ms.

I.7.7 PS1 restricted mode power-up

Refer to 9.10.2.

NOTE – Only required for power source intended to be compatible with an APS (see Figure I.9).



C Capacitor with value (Q × 25 µF)

FIGURE I.9/I.430

PS1 restricted mode compatible with APS

Connect the power source as shown in Figure I.9, with the APS switched on. Switch off the APS and monitor the voltage at the output of the power source. When the voltage is between +5 V and +2 V, the power source must switch to restricted mode, and the voltage must then fall within the limits indicated in Figure I.10.

I.8 APS Dynamic requirements

I.8.1 APS Switch-on time

Refer to 9.9.2.

Connect the APS as shown in Figure I.11. For an APS rated at P NPCUs, the load is resistive with a value such that it consumes (P + 4) NPCU at the normal output voltage of the APS; the additional 4 PCUs represents the power required to overcome the NT1 restricted mode power source. The capacitor shown represents the input capacitance of the TEs.

Apply input power to the APS and measure the rise-time of the output voltage using an oscilloscope. The rise-time must not exceed 2.5 ms measured between 1 V and 34 V at the output, and the output voltage must not fall below 34 V for a further 2.5 ms.

NOTE – It is acceptable for a time delay of up to 1 second to occur after the application of input power, before the output voltage starts to rise.

I.8.2 APS switch-off time

Refer to 9.9.3.

Set up the APS with a capacitive load of 100 nF (intended to simulate the typical cabling capacitance). Switch off the input power to the APS and measure the fall time of the output voltage using an oscilloscope.

NOTE – The input resistance of the oscilloscope together with its voltage probe must be at least 1 Mohm.

The fall time must not exceed 2.5 ms measured between 34 V and 1 V at the output, and the output voltage must not rise above 1 V for a further 2.5 ms.

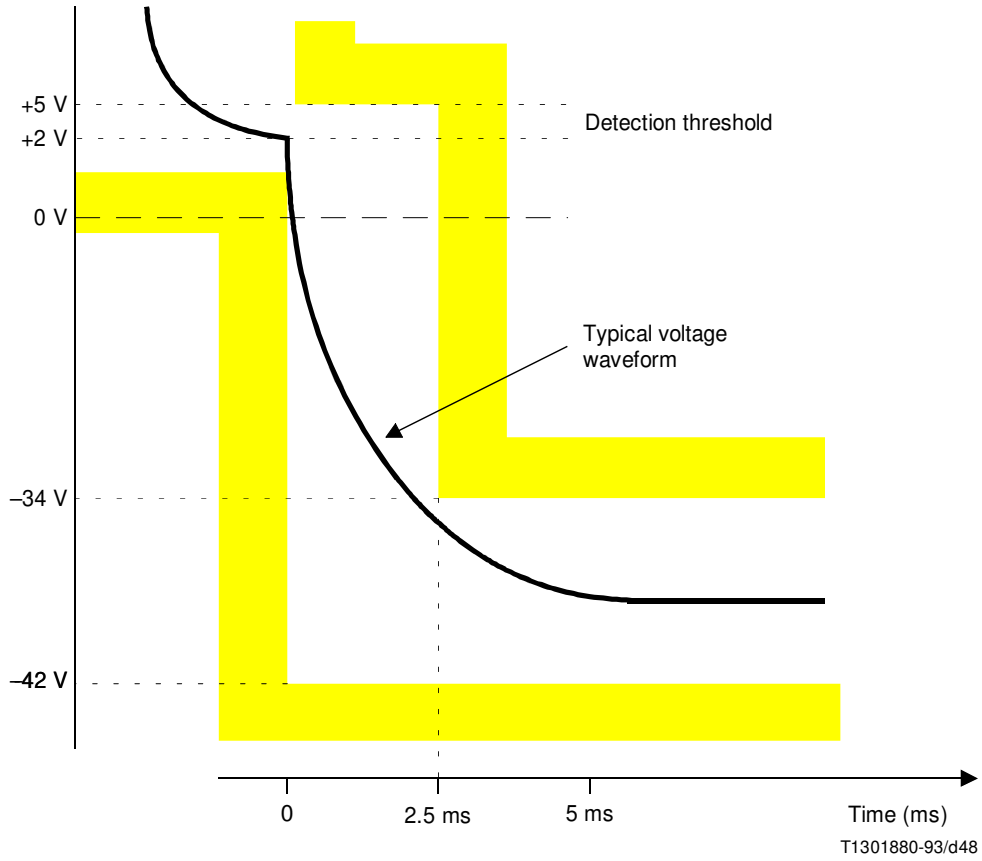


FIGURE I.10/I.430

PS1 output voltage at switchover from APS

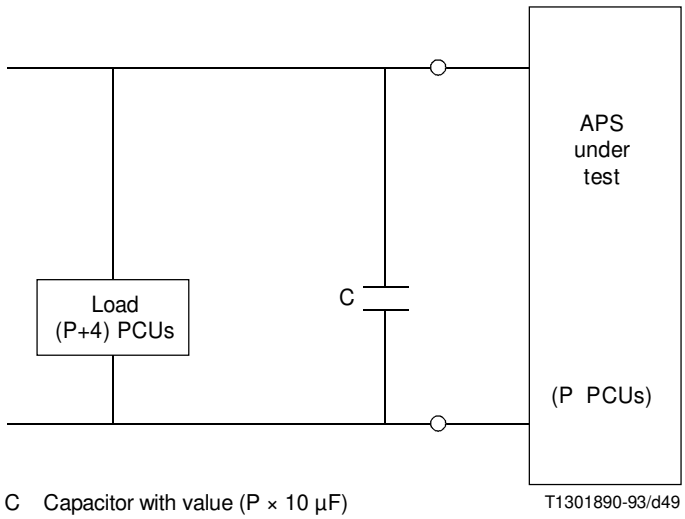


FIGURE I.11/I.430

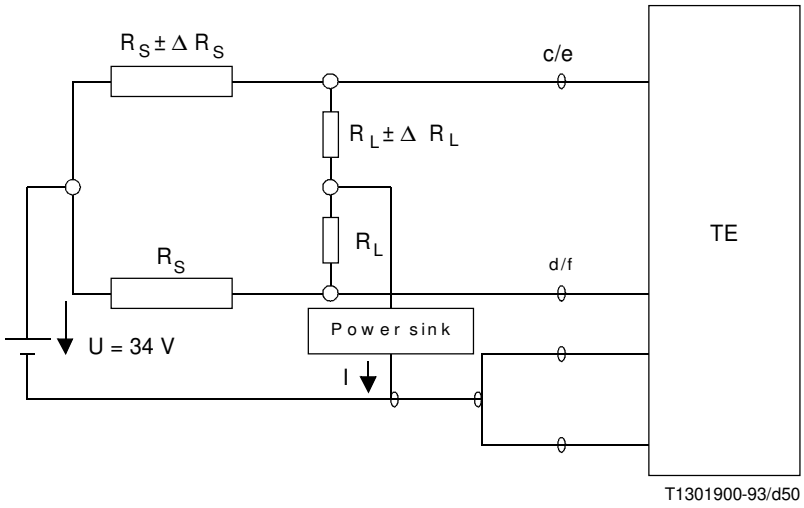
APS switch-on time measurement

I.9 Testing for current unbalance

Refer to 9.8

TE and NT equipment are expected to operate in multipoint configurations. In this configuration both TEs and NTs will experience DC imbalances caused by the equipment connected to the bus and the interconnecting wiring. To assure compatibility, the transformers in the TEs and NTs must avoid saturation over a range of DC imbalance and continue to meet the requirements specified in 9.8.1.2 and 9.8.2.2.

The test configurations shown in Figures I.12 and I.13 model the expected environment for TEs and NTs respectively. The resistor values represent the interconnecting wiring (R_S) and the combined TE cord and transformer resistance (R_L). The current through the load represents the TEs bridged across the unit under test.

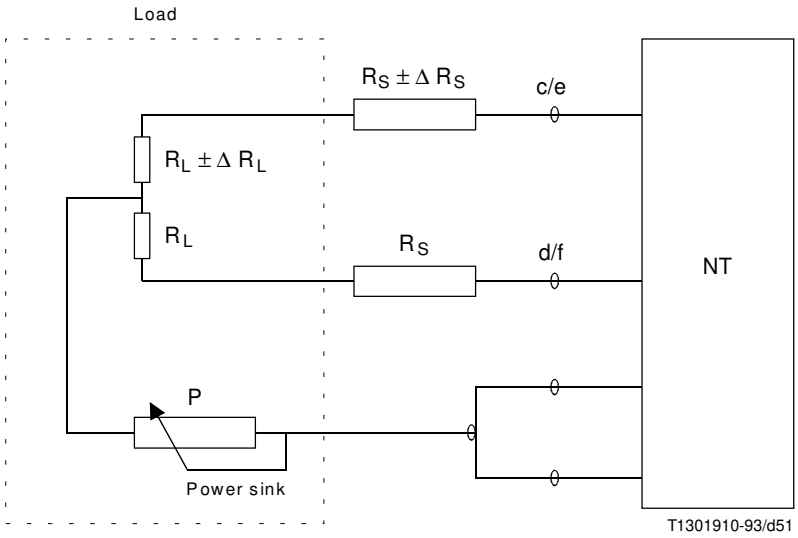


R_S = 6 ohms	ΔR_S = 360 Mohms
R_L = 5 ohms	ΔR_L = 300 Mohms

NOTE – The power sink should have a power consumption of either (80-N) PCUs or 40 PCUs, whichever is less, where N is the designated NPCU for the TE under test.

FIGURE I.12/I.430

Test circuit for impedance measurement of TE with applied current unbalance



R_S = 6 ohms	ΔR_S = 360 Mohms
R_L = 5 ohms	ΔR_L = 300 Mohms

NOTE – The load should be chosen so that it consumes the full rated output of the NT power source (i.e. P PCU), where P is the designated NPCU for the unit under test.

FIGURE I.13/I.430

Test circuit for impedance measurement of NT with applied current unbalance

Appendix II

Guidelines for implementation

(This appendix does not form an integral part of this Recommendation)

II.1 Power feeding

II.1.1 Introduction

This clause provides additional information for guidance in the design and application of terminals and/or power sources for use with PS1 (phantom power feeding). The information is intended to clarify the requirements given in the body of the Recommendation, and to give a rationale for some of the values and limits provided. It also includes some suggested methods whereby performance may be enhanced, to exceed the minimum level assured by the requirements given in 9.

Even though the details given in this clause refer primarily to PS1 power feeding, most of the principles also apply for PS2 power feeding, and should be taken into account when designing power sources, power sinks and wiring configurations using PS2.

Although it may be possible to have a configuration where both PS1 and PS2 are provided simultaneously, this is not expected to be a normal arrangement, and could in fact result in some power contention issues. For example, some terminals may be designed to operate from either PS1 or PS2 (whichever is available), and may therefore provide some internal connection between the access pairs used for the two power sources. If both sources were provided simultaneously, and one switched to restricted mode, there could then be a power contention.

II.1.2 Power consumption

II.1.2.1 Power consumption units

Power consumption units (PCU) have been used throughout 9 to define the power consumed by a TE as well as the power available from a PS1/2 power source. The rationale for using this PCU concept rather than simply referring to power in watts is as follows:

i) PS1 (and PS2) power is provided and consumed on the S-bus within closely defined limits of voltage, current, transient surges, etc. Use of the PCU concept implies that these factors have been taken into account, and makes it possible to express NT and TE powering characteristics as a single value, whereas multiple values would have been required in order to express it in watts.

ii) By rating power sources and sinks in terms of PCUs, the user can easily verify that his installation is workable from a powering viewpoint by performing a simple addition. Provided that the combined PCU rating of all the TEs on a bus is within the PCU rating of the source, the installation will be satisfactory.

iii) The use of well-defined units will ensure uniformity of rating between manufacturers.

iv) PCUs have been defined so as to cover both normal and restricted modes, and to allow for a difference in power (100 mW vs 95 mW) between modes.

II.1.2.2 Terminal power consumption

Terminals should be designed to minimize power consumption as much as possible, particularly for a terminal providing only a basic telephony service, where the power should not normally exceed 10 NPCUs. If the rated NPCU of the terminal is greater than 10, portability cannot be guaranteed since the minimum power available from the NT1 may be only 10 NPCUs in some cases.

Even for terminals providing complex additional functionality, power consumption should not normally exceed 40 NPCUs, although a maximum up to 80 NPCUs may be permissible in exceptional cases.

II.1.2.3 Power available

It is important to realize that power is defined in terms of the power available at the TE, and this must be taken into account when designing a power source and when planning a bus configuration. The DC resistance of the bus wiring is relatively high in most cases, and significantly increases the amount of power which the PS1 source must provide. (In the case of PS2, the wiring resistance will typically be twice as high as for PS1, since only a single wire pair is employed, making the effect even more important).

When considering transient interworking, the wiring resistance is again very significant, as any surge currents will be higher than the DC current. Care must be taken to avoid a potential “power lock-up” condition due to the high source impedance (wiring resistance plus current limiting of the source) in conjunction with the negative input impedance of the DC-to-DC converter in the TE. Refer to the clauses on dynamic interworking in this appendix (see II.1.5) and in the body of the Recommendation (see 9.7).

II.1.3 General assumptions

The requirements for the power source and the power sink during transient conditions (see 9.7) have been derived using “typical” configurations, and do not attempt to fully cover multiple worst-case situations. For example, it is unlikely that all TEs on a bus will simultaneously draw the maximum permitted current surge for the maximum time allowed, and the requirement for the surge capability of the source takes this into account.

Similarly, the allowance made for voltage drop in the bus wiring when deriving the current surge requirements has not considered the maximum loop length, maximum wiring resistance, maximum load (all TEs at the end of the bus, and all drawing full rated PCUs) and minimum source voltage all occurring simultaneously.

II.1.4 Power source ripple

The power source must be designed so that its output ripple does not interfere with proper operation of the TEs on the bus. As a guideline to ensure this, the ripple voltage should not exceed 1 V RMS (or 3 V peak-to-peak) under any conditions of operation up to the rated maximum PCUs of the source. However, EMI considerations may further limit the acceptable ripple to a level below this figure.

II.1.5 Dynamic behaviour of power sources and sinks

II.1.5.1 Need for dynamic interworking

There are several distinct circumstances which require that the sink and source be capable of dynamically interworking, and it is helpful to separate them to clarify the requirements for each case. The conditions to be addressed include:

- power-up in normal mode;
- power-up in restricted mode;
- switchover from normal to restricted mode;
- switchover from restricted to normal mode;
- addition of a TE during operation in normal mode;
- addition of a TE during operation in restricted mode.

Each of these cases has been addressed by one or more of the various requirements for dynamic interworking given in this Recommendation.

II.1.5.2 Power-up and recovery from short-circuit

During power-up all power sources and sinks are in a well defined initial state. All capacitors are discharged, any timing circuits are reset, software/firmware is initialized, and there are no calls in progress.

Definition of dynamic requirements for this phase include power source requirements for rise-time and surge capability, and power sink (TE) requirements for surge current, power consumption and behaviour at low input voltage.

II.1.5.3 Switchover

During switchover from restricted to normal mode, a non-designated TE will go through a normal power-up sequence, and it is important that this does not cause a designated TE to lose a call. This leads to the requirements for power source switchover time, and for TE holdover time.

II.1.5.4 Addition of a TE

At the instant that a TE is added to an operating bus, it is important that any other TEs on the bus do not lose calls. This gives rise to additional surge requirements for the power source.

II.1.5.5 Summary of PS1 dynamic requirements

The various requirements for dynamic interworking as defined in this Recommendation are summarized in Table II.1.

TABLE II.1/I.430

Dynamic power requirements

Condition	Source requirements	Sink requirements
Power up (normal mode)	< 350 ms rise-time, 1V to 34 V > P × 3 mA at 34 V > P × 4.5 mA for 100 ms	Must be compatible with the source rise-time of 350 ms N × 100 mW max, 24V to 42 V 55 mA max for 100 ms
Power up (restricted)	< 1.5 s rise-time, 1V to 34V > 9 mA at 1V > Q × 2.75 mA at 34V (no surge specified)	Must be compatible with the source rise-time of 1.5 s 380 mW max, 32 V to 42 V 11 mA from 40 V // 300 µF 9 mA from 40 V 55 mA max for 100 ms
Switchover (normal to restricted)	Time < 5 ms > 9 mA at 1 V > (Q × 2.75) mA at 34 V	Holdover > 5 ms (M × 2.75) mA from 40 V source
Switchover (restricted to normal)	Time < 5 ms > P × 4.5 mA for 100 ms with voltage not below 30 V	Holdover > 5 ms (+ power up requirements for non-designated TE)
Add TE to bus (normal)	50 mA surge for 100 ms with V not below 34 V	55 mA max for 100 ms 24 V minimum
Add TE to bus (restricted)	50 mA surge for 100 ms with V not below 34 V (battery source only)	55 mA max for 100 ms 32 V minimum

II.1.5.6 Requirements for interworking

Considering all the above, and related issues, the overall objective for the power source/sink dynamic behaviour has to be clearly stated. Several levels of functionality during transient conditions are possible:

1) no power lock-up condition, i.e. all TEs eventually recover normal operation;

2) no loss of call in progress;

3) no audible disturbance to a telephony call;

4) no bit errors on the data stream;

5) etc.

The first level is mandatory for all applications, and every effort must be made to ensure that the second level is also met except under extreme worst-case conditions. The implementation must therefore meet these basic criteria (1 and 2 above), but depending on the level of additional functionality required, the implementation for certain applications may be more complex as it affects the TE and/or the power source in order to provide for meeting 3) and 4) above.

Possible design improvements for the power source and the TE, to meet this extended functionality, are given in II.1.6 and II.1.7.

II.1.5.7 TE start-up considerations

The passive bus is a complex configuration as regards to the interworking of power source 1 with multiple power sinks. The most critical condition occurs after the removal of a short-circuit in the interface installation, when the power source 1 may be overloaded unless the TE input capacitors have been charged and the DC-to-DC converters have started operating.

Therefore the TE power start-up behaviour needs to be controlled to allow the power source to recover from the overload condition and to restore the required surge capability. The requirements for the TE depend on a number of independent aspects and characteristics:

Power source 1 aspects:

– deliverable power in NPCU;

– output voltage with load;

– implementation of current surge capability;

– overload and short-circuit protection.

TE (power sink 1) aspects:

– power consumption during start-up;

– power consumption during operational state;

– the way in which the DC-to-DC converter switches on (e.g. input voltage level detection or timer; hard or soft start; etc.)

– input current limiter level;

– effective input capacitance.

Configuration aspects:

– number of TEs using phantom power connected to the bus;

– power consumption in NPCU of each of the TEs connected;

– operational status of each TE;

– power loss on the interface wiring.

It is unlikely that for all aspects the worst-case condition may be present at the same time, and to take full account of this possibility would create an unnecessary burden for the implementation of power sources and sinks. On the other hand, it is not possible to define the requirements for the TE without consideration of the interworking with the source and the other sinks. A test arrangement for a TE has therefore been designed taking into account the arguments above which is considered to assure compatibility of TEs using power sink 1 in real configurations. If a number of aspects may be close to worst case in real configurations it will not result in a power lock-up situation, but may possibly cause some delay in powering up of one or more TEs.

Based on the above considerations, terminal requirements are given in 9.7.3.1, and a test method is described in I.6.

II.1.6 Power source design for improved performance

II.1.6.1 Surge time

A power source (PS1) designer may choose to improve the performance beyond the minimum guaranteed by the parameters given in this Recommendation, by designing for increased surge capability (current and/or time) to cover the multiple worst-case conditions suggested in II.1.2. In this case, a current surge capability of P × 5.5 mA for 150 ms under start-up conditions should be considered (see 9.7.2 and 9.7.4).

II.1.6.2 Switchover time

The power source may be designed to remain in restricted polarity for a minimum time (10 seconds is suggested, to correspond with the TE requirement given in 9.7.3.2) before switching to normal polarity, to avoid potential problems due to rapid switching back and forth between polarities. Any such rapid switching could discharge the energy storage capacitor in the TE to the point where the TE no longer has sufficient holdover to either transmit the required primitives indicating loss of power (for a non-designated TE) or else to avoid losing an ongoing communication (for a designated TE).

II.1.7 TE design for improved performance

There are two possible options to reduce any potential disruption caused by connecting a TE to the bus: first, the TE surge current may be delayed for a short period after the TE is connected; alternatively, the TE may be designed so that it does not draw any surge current in excess of the normal operating current.

II.1.7.1 Delayed TE surge current

To achieve the first objective, the current-time mask for a TE (see Figure 23) may be revised in accordance with Figure II.1. Tables 12 and 13 would also be revised, as given in Tables II.2 and II.3 below. This revised mask permits the implementation of a delay time (B in Tables II.2 and II.3) between connection to the bus and the terminal start-up current surge. Such a delay allows time for all pins of the connector to make contact, thereby avoiding the possibility of disrupting the operation of other TEs due to transient current imbalance through a momentary 3-wire connection.

NOTE – Figure II.1 is drawn to illustrate a typical terminal. For some high-power terminals (power consumption greater than approximately 22 NPCUs), the current X will be greater than the current Y.

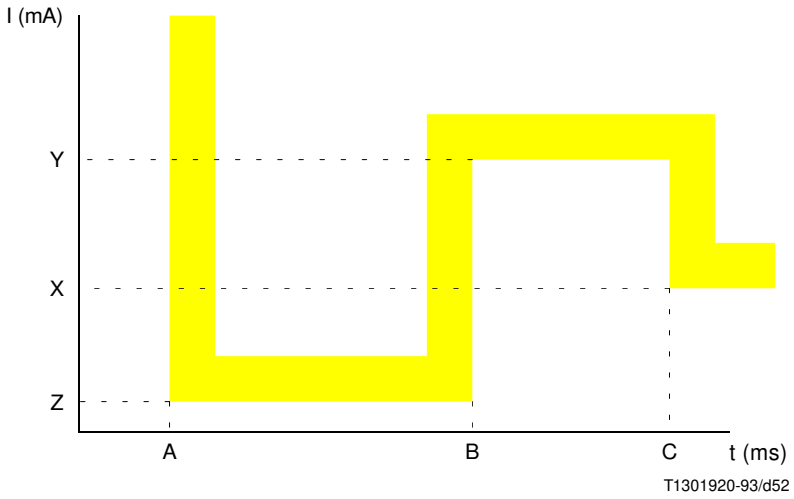


FIGURE II.1/I.430

TE current time mask (revised)

TABLE II.2/I.430

Parameters for TE in normal mode (revised)

Timing limits	Current limits
A = 5 µs	Z = 4 mA
5 µs < B < 900 ms	Y = 55 mA or, for N < 10, (N × 5.5) mA
C = B + 100 ms	X = Current equivalent to NPCU of TE

TABLE II.3/I.430

Parameters for TE in restricted mode (revised)

Timing limits	Current limits
A = 5 µs	Z = 4 mA
5 µs < B < 900 ms	Y = (M × 14) mA
C = B + 100 ms	X = Current equivalent to RPCU of TE

II.1.7.2 Reduced TE surge current

II.1.7.2.1 TE Design to minimize power disturbance

To improve the performance of a TE for power transient conditions (connection, switch-on and switch-over between normal and restricted modes), consideration should be given to further limiting the TE transient current within the mask given in 9.4.1. By appropriate design of the TE, the transient current can be effectively eliminated, keeping its value below the steady-state current drawn by the TE. The revised current/time mask is shown in Figure II.2 for normal mode and in Figure II.3 for restricted mode. Note that these masks could be combined with that given in II.1.7.1 above, to allow for a delay time between connection to the bus and terminal start-up.

II.1.7.2.2 TE Input capacitance

Other TE requirements would remain unchanged, except that the maximum effective capacitance limit should be reduced from 100 µF to 2 µF. This 2 µF limit is for capacitance measured directly at the PS1 input to the TE. Additional capacitance required to meet the holdover requirements must be implemented so that it does not appear directly at the PS1 input, but can still provide power for the DC-to-DC converter when needed. A possible implementation is suggested in Figure II.4.

II.1.7.2.3 Power source implications

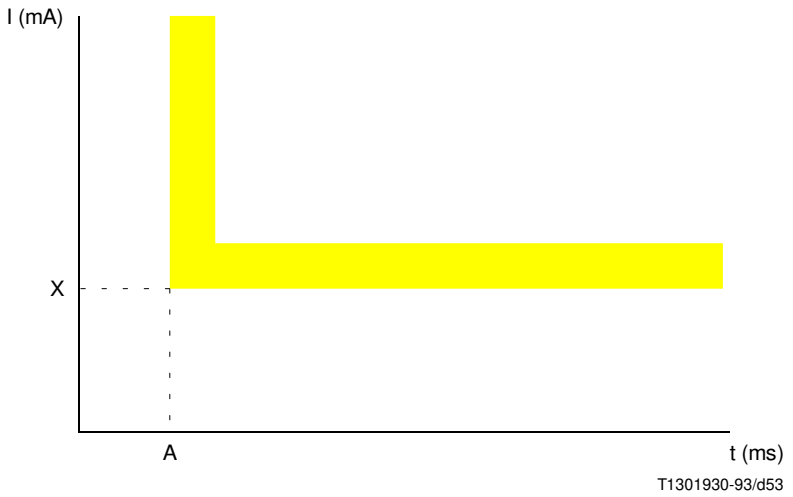
The TE discussed above will be fully capable of interworking with the power source as described in 9.4.4. TEs meeting either specified limit can therefore be mixed within the same network and will provide basic functionality.

Furthermore, if all TEs connected to a given NT1 comply with the limits suggested above, then all TEs will potentially offer improved functionality during transient conditions. In addition, some of the power source requirements listed in 9.4.4 could be simplified although in this case, the power source may reduce the interworking capability with terminals following the template given in 9.4.1.

II.2 Information on activation and deactivation tables

The requirements on activation and deactivation contained in 6.2.3 are supplemented by Tables 5 C.1 and C.2. These tables provide examples of compatible implementation alternatives. This information is provided to assist the designer in selecting the most appropriate procedure for a specific type of equipment.

In most cases the state transitions are the logical result of the activation and deactivation procedures. However, the operation of Timer T3 and the choice of transitions contained in Notes 5 and 6 of Table C.2 may require additional rationale for the intended operation.

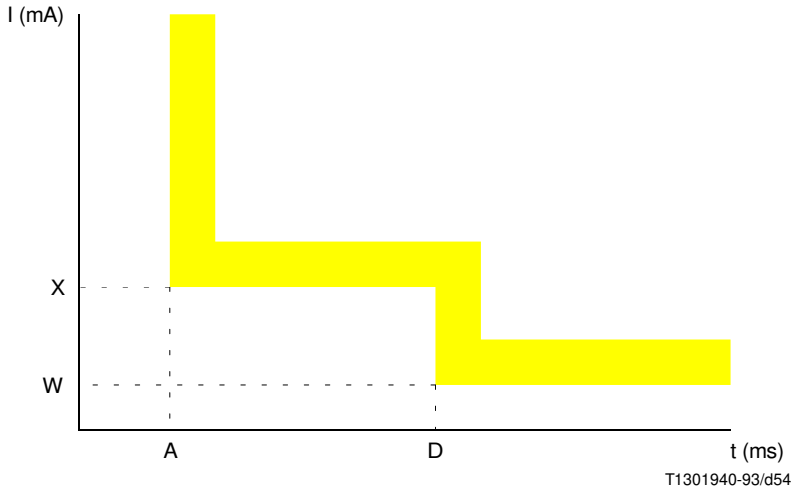


A = 5 µs

X = Current equivalent to NPCUs of TE

FIGURE II.2/I.430

Suggested current time limitation for TE in normal mode



A = 5 µs

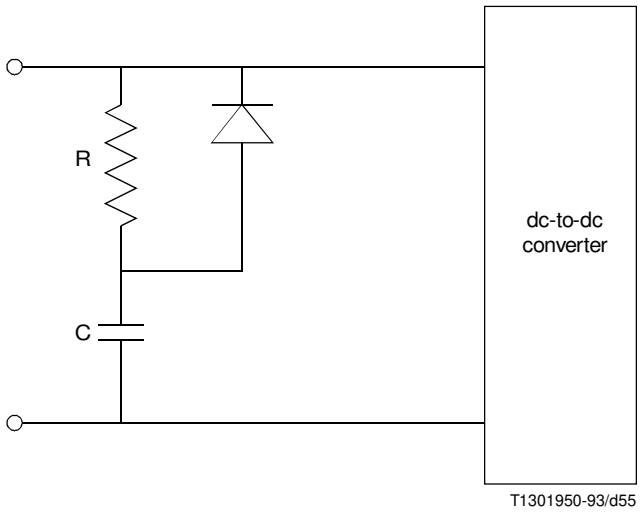
D = 10 ms

X = Current equivalent to NPCUs of TE

W = Current equivalent to RPCUs of TE

FIGURE II.3/I.430

Suggested current time limitation for TE in restricted mode



C Holdover capacitor
R Charging resistor

FIGURE II.4/I.430

TE holdover capacitor

II.2.1 Operation of Timer T3

The expiry of Timer T3 is intended to provide an indication that the network side cannot complete the activation procedure, probably due to a failure condition or the terminal cannot detect INFO 4. Timer T3 is stopped and reset when the TE reaches the activated state (F7). Upon the expiry of T3, the TE goes to the deactivated state (F3) unless it is in the synchronized state (F6). The TE remains in state F6 rather than going to F3 for the following reasons:

1) The TE is receiving INFO 2 and a transition to F3 would return the TE to state F6 without re-starting T3. The result of this dual state change is a return to the original state.

2) The transition through F3 cannot be verified and cannot be tested.

3) When the TE is in a multipoint configuration, a transition to F3 (sending INFO 0) would have no meaning if the network is receiving INFO 3 from another TE on the bus.

4) The higher layers of the network side may recognize that full activation has not been achieved and can initiate management procedures to resolve the status of the access line.

II.2.2 Connection status

The activation and deactivation procedure for a locally powered TE able to detect power source 1 or 2 is contained in Table C.2. Two possible implementations are described in Notes 5 and 6.

In the first case, the TE detects the presence of INFO 2 or INFO 4 plus the presence of the interface power source to determine its connection status. This implementation disconnects from the interface only when both events “power S not detected” and “receiving INFO 0” are detected at the same time. This allows the TE to maintain its connected status in the event that the interface power source is below the selected threshold value and the TE is still receiving a valid INFO 2 or INFO 4 signal.

The second case uses only the detection of the interface power source to determine its connection status and disconnects from the interface when the interface power source is below the selected threshold.