FIGURE 2/G.812

Permissible maximum relative time interval error (MRTIE) due to long-term phase variations vs. observation period S for a slave clock under holdover operation

1) For $S \geq 100$, $MRTIE(S) = (aS + 1/2\ bS^2 + C)$ ns
where parameters a, b, c are proposed provisionally as (Note 5):

TABLE 1/G.812

	Transit Clock	Local Clock
a	0.5 (1)	10.0 (3)
b	1.16×10^{-5} (2)	2.3×10^{-4} (4)
c	1000 (6)	1000 (6)

Note 1 - Corresponds to an initial frequency offset of 5×10^{-10}

Note 2 - Corresponds to a frequency drift of 1×10^{-9}/day.

Note 3 - Corresponds to an initial frequency offset of 1×10^{-8}

Note 4 - Corresponds to a frequency drift of 2×10^{-8}/day

Note 5 - Temperature effects: the effect of changes in environmental temperature on the performance of a slave clock in holdover mode requires further study.

Note 6 - Takes care of any MRTIE that might have existed at the beginning of holdover operation, and of effects of internal reconfiguration, etc. in the clock (and timing distribution, if applicable). In any case, a smooth transition between "ideal" and "holdover" operations is stipulated.

The resultant overall specification is summarized in Figure 2/G.812.

2.3 Short-term phase variations

Clock implementations exist which may have some high frequency phase instability components. The maximum permissible short-term phase variation of a slave clock due to jitter is under study.

FIGURE 1/G.812

Permissible maximum relative time interval error (MRTIE)
due to long-term phase variations vs. observation
period S for a slave clock under ideal operation

Note - For measurement of long-term variations the use of a 10 Hz low-pass filter with a 20 dB/dec roll-off is suggested.

2.2.3 Holdover operation

This category of operation reflects the performance of a clock for the infrequent times when a slave clock will lose reference for a significant period of time.

The MRTIE (see item 1.2 and Recommendation G.811) at the output of the slave clock should not, over any period of S seconds, exceed the following provisional limits.

exceed 1/8 UI up to a total amount of 1 us.

Where the UI corresponds to the reciprocal of the bit rate of the interface.

2.2 Long-term phase variations

Slave clock phase stability requirements must account for clock behaviour in real network environments. Impairments such as jitter, error bursts, and outages are intrinsic characteristics of timing distribution facilities. The following specifications are based on the slave clock phase stability model contained in the Annex. This model characterizes actual clock performance, reflecting the stress conditions in real networks under which clocks should perform acceptably. There are three categories of clock operation which require specification:

i) ideal,

ii) stressed, and

iii) holdover.

2.2.1 Ideal operation

This category of operation reflects the performance of a clock under conditions in which there are no impairments on the input timing reference(s).

The MRTIE at the output of the slave clock should not, over any period of S seconds, exceed the following provisional limits:

1) $0.05 < S < 100$: this region requires further study;

2) 1000 ns for $S \geq 100$.

The resultant overall specification is summarized in Figure 1/G.81x.

2.2.2 Stressed operation

This category of operation reflects the actual performance of a clock considering the impact of real operating (stressed) conditions. Stressed conditions include the effects of jitter, protection switching activity, and error bursts. The result of such stressed conditions is timing impairments, as discussed in the annex.

The requirements for stressed operation are under study.

4.Recommendation G.812

TIMING REQUIREMENTS AT THE OUTPUTS OF SLAVE CLOCKS SUITABLE FOR PLESIOCHRONOUS OPERATION OF INTERNATIONAL DIGITAL LINKS

1.General

1.1Purpose of this Recommendation

The purpose of this Recommendation is to specify requirements for slave clocks, and promote understanding of associated timing requirements for plesiochronous operation of international digital links.

Note - Administrations may apply this Recommendation, at their own discretion, to slave clocks other than those used in connection with international traffic.
Supplement No. 35 gives guidance on one suitable method for the measurement of clock performance with respect to this Recommendation.

1.2Maximum relative time interval error

The concept of maximum relative time interval error (MRTIE) is useful in specifying slave clock performance. MRTIE is analogous to MTIE as defined in Recommendation G.811 but with reference to a practical high-performance oscillator instead of UTC.

2.Phase stability of slave clocks

The phase stability of a slave clock can be described by its phase variations which in turn can be separated into a number of components:

- phase discontinuities due to transient disturbances;

- long-term phase variations (wander and integrated frequency departure);

- short-term phase variations (jitter).

A phase stability model for slave clocks is described in the Annex to this Recommendation.

2.1Phase discontinuity

In cases of infrequent internal testing or rearrangement operations within the slave clock, the following conditions should be met:

- the phase variation over any period up to 2^{11} UI should not exceed 1/8 of a UI;

- for periods greater than 2^{11} UI in the phase variation for each interval or 2^{11} UI should not