INTERNATIONAL TELECOMMUNICATION UNION

ITU-T G.804

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

(11/93)

DIGITAL NETWORKS

ATM CELL MAPPING INTO PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

ITU-T Recommendation G.804

(Previously "CCITT Recommendation")

FOREWORD

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ITU-T Recommendation G.804 was prepared by ITU-T Study Group 13 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 26th of November 1993.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Recommendation G.804

ATM CELL MAPPING INTO PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

(Geneva, 1993)

1 Introduction

This Recommendation identifies the way of transporting ATM cells over PDH networks at different hierarchical bit rates.

1.1 Scope

Existing transmission networks are based on Plesiochronous Digital Hierarchy (PDH) as defined in Recommendation G.702. ATM is considered as the suitable technique to support B-ISDN. The Synchronous Digital Hierarchy (SDH) will form the basis of transport of the ATM cells.

During the transition period, there are needs to transport ATM cells using existing PDH transmission networks. This Recommendation provides the mapping to be used for this transport of ATM cells on the different PDH bit rates for both 1544 and 2048 kbit/s hierarchies.

1.2 Abbreviations

For the purposes of this Recommendation, the following abbreviations apply:

AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode
B-ISDN	Broadband aspects of Integrated Services Digital Network
BIP-8	Bit Interleaved Parity-8
CRC	Cyclic Redundancy Check
FEAC	Far End Alarm and Control
FEBE	Far End Block Error
FERF	Far End Receive Failure
HEC	Header Error Control
LOC	Loss of Cell delineation
OAM	Operation, Administration and Maintenance
PDH	Plesiochronous Digital Hierarchy
PLCP	Physical Layer Convergence Protocol
POH	Path OverHead
POI	Path OverHead Identifier
SDH	Synchronous Digital Hierarchy
RAI	Remote Alarm Indication
TS	Time Slot

1.3 Definitions

For the purposes of this Recommendation, the following definitions apply:

idle cell: A cell which is inserted and extracted by the physical layer in order to adapt the cell flow rate at the boundary between the ATM layer and the physical layer to the available payload capacity of the transmission used.

valid cell: A cell whose header has no errors or has been modified by the cell Header Error Control (HEC) verification process.

nibble: A nibble is a group of four bits.

NOTE – The order of transmission of information in all diagrams in this Recommendation is first from left to right and then top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left of all diagrams.

2 Mapping of ATM cells into 1544 kbit/s

2.1 Frame format

The multiframe structure for the 24 frame multiframe as described in Recommendation G.704 shall be used.

The ATM cell is mapped into bits 2 to 193 (i.e. time slots 1 to 24 described in Recommendation G. 704) of the 1544 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 2-1).

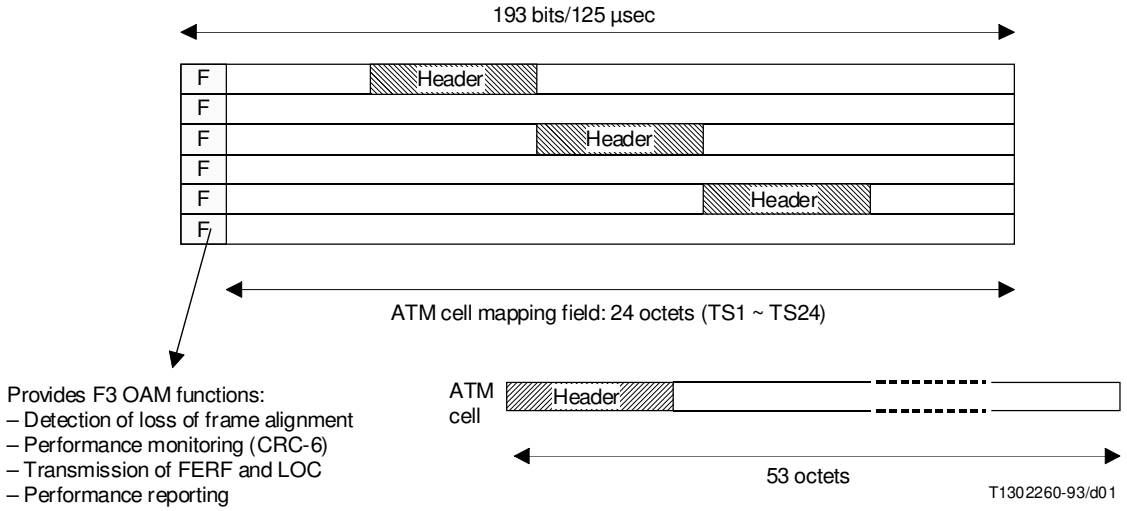


FIGURE 2-1/G.804

Frame structure for 1544 kbit/s used to transport ATM cells

2.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

2.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.

2.4 Scrambling of the ATM cell payload (optional)

As an option the ATM cell payload (48 bytes) can be scrambled before mapping into the 1544 kbit/s signal. If this option is used, then, the reverse operation, following termination of 1544 kbit/s signal, the ATM cell payload will be descrambled before being passed to ATM layer. The self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432, is used. If this option is not used, then no descrambling is done in the reverse operation.

2.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.

2.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

2.7 Physical layer OAM

The error detection and performance reporting functions described in Recommendation G.704 are used. In addition, the loss of cell delineation (LOC) is to be reported by a priority data link message. The specific 16-bit codeword is for further study.

3 Mapping of ATM cells into 2048 kbit/s

3.1 Frame format

The basic frame structure at 2048 kbit/s as described in Recommendation G.704 shall be used.

The ATM cell is mapped into bits 9 to 128 and bits 137 to 256 (i.e. time slots 1 to 15 and time slots 17 to 31 described in Recommendation G. 704) of the 2048 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 3-1).

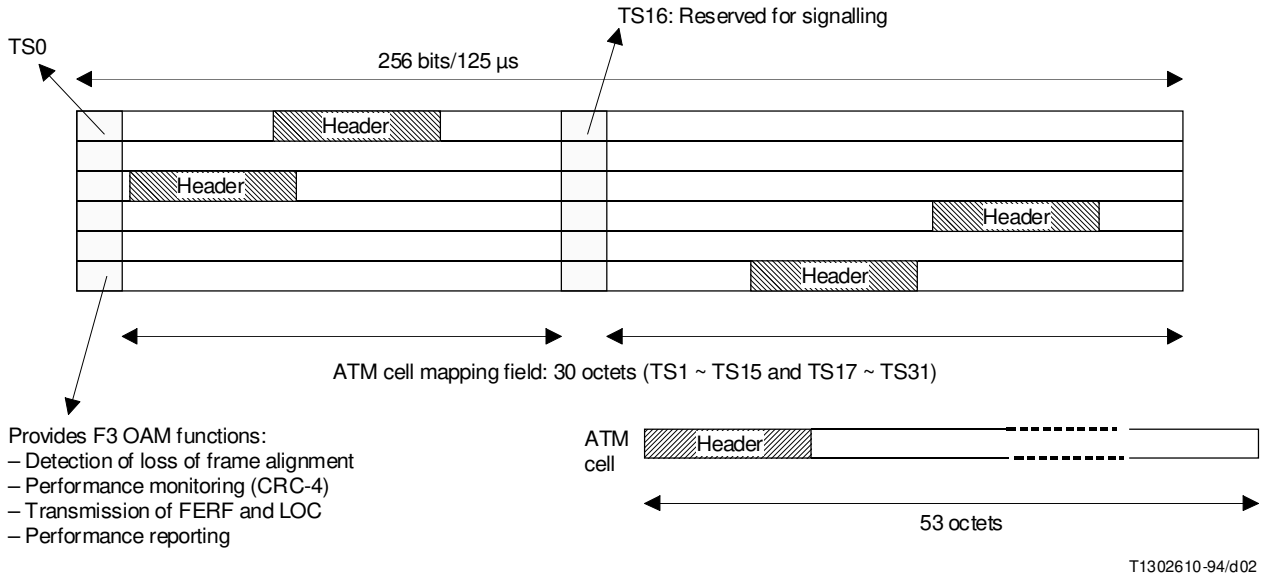


FIGURE 3-1/G.804

Frame structure for 2048 kbit/s used to transport ATM cells

3.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

3.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.

3.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 2048 kbit/s signal. In the reverse operation, following termination of 2048 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 2048 kbit/s frame alignment word.

3.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.

3.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

3.7 Physical layer OAM

The error performance monitoring is performed by the CRC-4 procedure defined in Recommendation G.706. The reporting of the FEBE, FERF and LOC are performed by dedicated bits in time slot zero of the frame structure.

4 Mapping of ATM cells into 6312 kbit/s

4.1 Frame format

The basic frame structure at 6312 kbit/s as described in Recommendation G.704 shall be used.

The ATM cell is mapped into bits 1 to 768 (i.e. time slots 1 to 96 described in Recommendation G.704) of the 6312 kbit/s frame with the octet structure of the cell aligned with the octet structure of the 6312 kbit/s frame. Bits 769 to 784 (time slots 97 and 98) are reserved for user communication channels and the last five bits (F-bits) are used for frame alignment and OAM (see Figure 4-1).

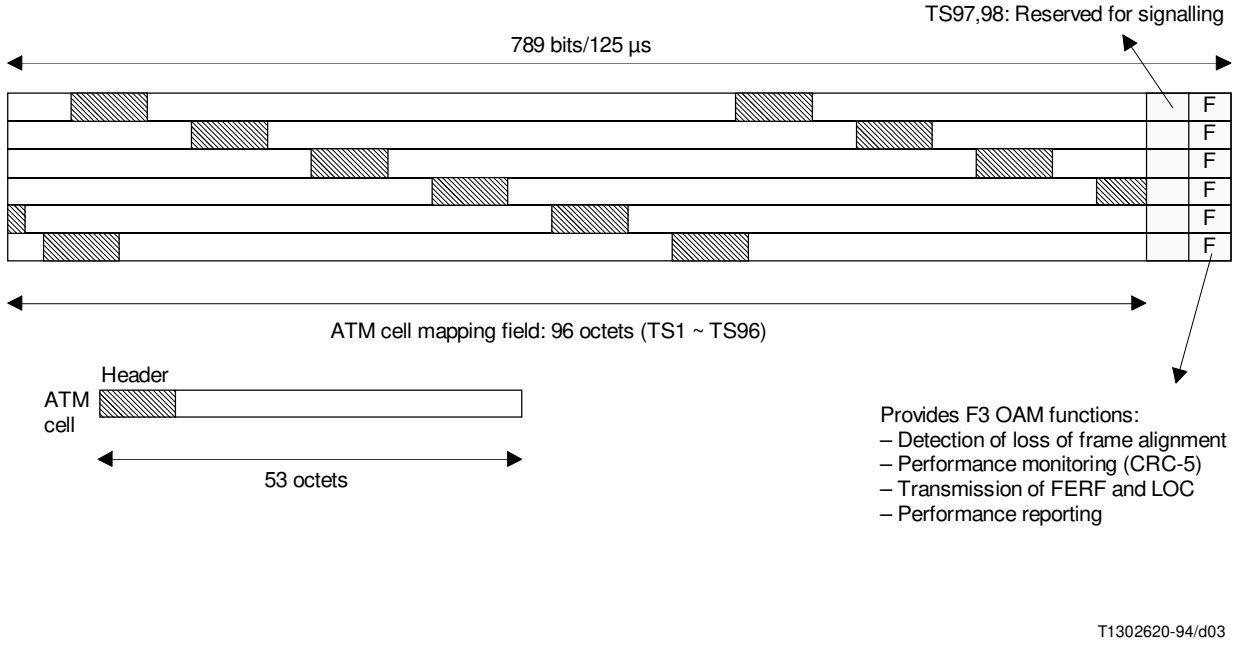


FIGURE 4-1/G.804

Frame structure for 6312 kbit/s used to transport ATM cells

4.2 Cell rate adaption

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

4.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.

4.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 6312 kbit/s signal. In the reverse operation, following termination of 6312 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 6312 kbit/s frame alignment word.

4.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.

4.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

4.7 Physical layer OAM

The error monitoring is performed by the CRC-5 procedure defined in Recommendation G.706. The transmission of the FERF is performed using the F-bits as described in Recommendation G.704. The FERF should also be used to indicate the LOC. The transmission of FEBE is for further study.

5 Mapping of ATM cells into 8448 kbit/s

For further study.

6 Mapping of ATM cells into 34 368 kbit/s

6.1 Frame format

The basic frame structure at 34 368 kbit/s as described in Recommendation G.832 shall be used.

The ATM cells are mapped into the 530 payload octets of the 34 368 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 6-1).

6.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

6.3 Header Error Control (HEC)

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.

6.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 34 368 kbit/s signal. In the reverse operation, following termination of 34 368 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and the replication of the 34 368 kbit/s frame alignment word.

6.5 Cell delineation

The cell delineation shall be performed using the HEC mechanism as defined in Recommendation I.432.

6.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

6.7 Physical layer OAM

Overhead bytes for physical layer OAM functionality are defined in Recommendation G.832.

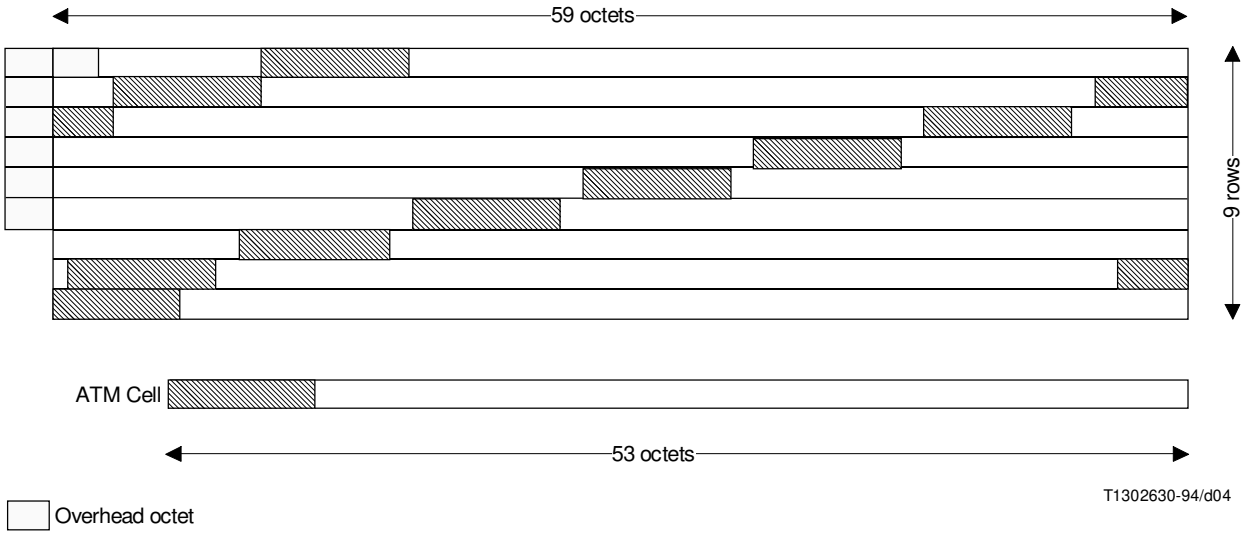


FIGURE 6-1/G.804

Frame structure for 34 368 kbit/s used to transport ATM cells

7 Mapping of ATM cells into 44 736 kbit/s

7.1 Frame format

The multiframe format at 44 736 kbit/s, as described in Annex A, shall be used.

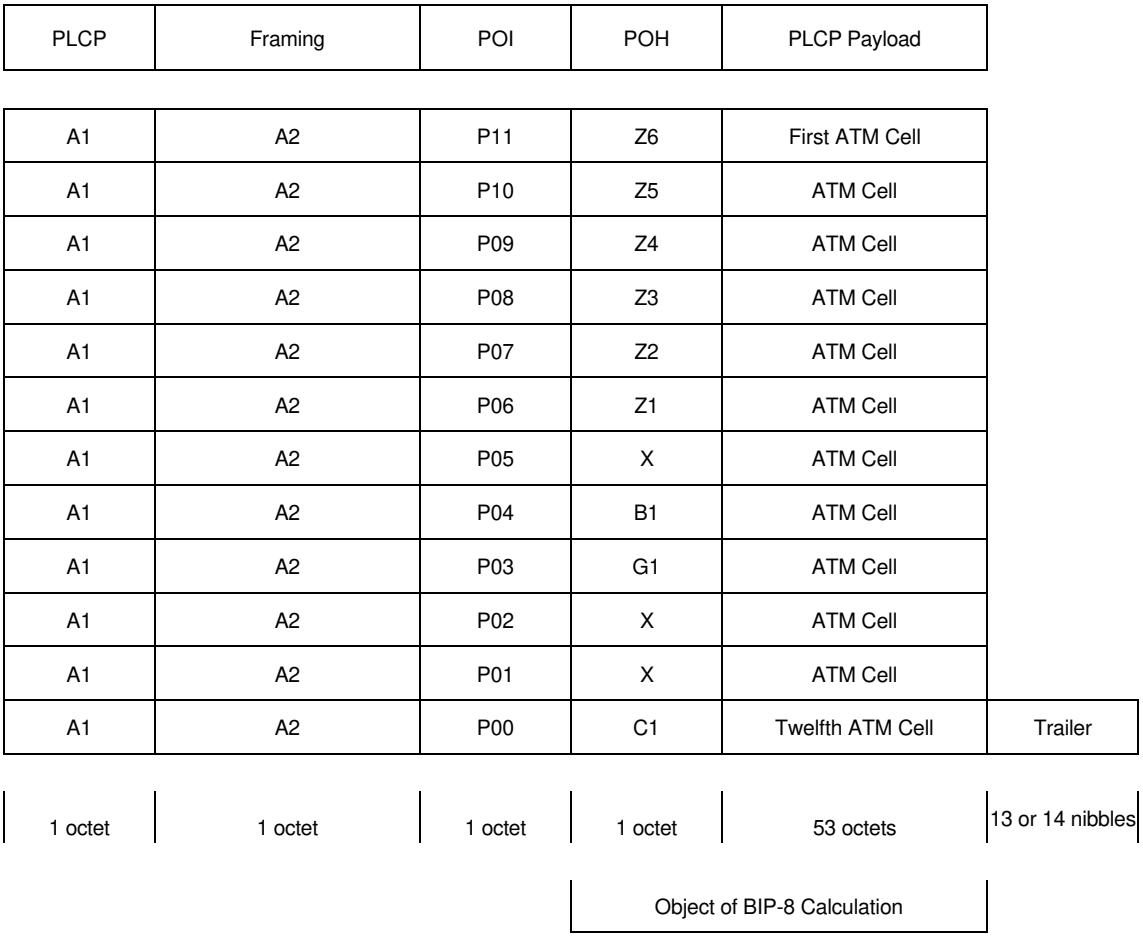
7.2 PLCP-based mapping of ATM cells

The ATM Physical Layer Convergence Protocol (PLCP) defines a mapping of ATM cells onto existing 44 736 kbit/s facilities. This PLCP is described in the following subclauses.

The PLCP consists of a 125 µs frame within a standard 44 736 kbit/s payload. Note there is no fixed relationship between the PLCP frame and the 44 736 kbit/s frame, i.e. the PLCP begins anywhere inside the 44 736 kbit/s payload. The PLCP frame, Figure 7-1 consists of 12 rows of ATM cells, each preceded by four octets of overhead. Nibble

stuffing is required after the twelfth cell to fill the 125 µs PLCP frame. Although the PLCP is not aligned to the 44 736 kbit/s framing bits, the octets in the PLCP frame are nibble aligned to the 44 736 kbit/s payload envelope. Nibbles begin after the control bits (F, X, P, C or M) of the 44 736 kbit/s frame. Note that the stuff bits are never used in the 44 736 kbit/s, i.e. the payload is always inserted. Octets comprising the PLCP frame are described in the following subclauses.

Note that order and transmission of all PLCP bits and octets are from left to right and top to bottom. The figures represent the most significant bit (MSB) on the left and the least significant bit (LSB) on the right.



POI Path Overhead Indicator
POH Path Overhead
BIP-8 Bit Interleaved Parity-8
X Unassigned – Receiver required to ignore

FIGURE 7-1/G.804

PLCP frame (125 µs)

7.2.1 Cell rate adaptation

The cell rate adaptation to the payload capacity of the PLCP frame is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

7.2.2 Header Error Control (HEC) generation

The HEC generation shall be compliant with Recommendation I.432.

7.2.3 Cell delineation

Since the cells are in predetermined locations within the PLCP, framing on the 44 736 kbit/s signal and then on the PLCP is sufficient in order to delineate cells.

7.2.4 Cell header verification and extraction

The cell header verification shall be compliant with Recommendation I.432. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

7.2.5 Physical layer OAM

7.2.5.1 PLCP overhead utilization

The following PLCP overhead bytes/nibbles are required to be activated across the UNI:

- A1 Frame alignment
- A2 Frame alignment
- B1 PLCP path error monitoring
- C1 Cycle/stuff counter
- G1 PLCP path status
- Px Path overhead identifier
- Zx Growth octets
- Trailer nibbles

7.2.5.2 Frame alignment (A1, A2)

The PLCP framing octets use the same framing pattern as used in the SDH. These octets are defined as A1 = 11110110, A2 = 00101000.

7.2.5.3 PLCP path error monitoring (B1)

The Bit Interleaved Parity-8 (BIP-8) field supports path error monitoring, and is calculated over a 12 × 54 octet structure consisting of POH field and the associated ATM cells (648 octets) of the previous PLCP frame.

7.2.5.4 Cycle/stuff counter (C1)

In general, the cycle/stuff counter provides a nibble stuffing opportunity cycle and length indicator for the PLCP frame. A stuffing opportunity occurs every third frame of a three frame (375 µs) stuffing cycle. The value of the C1 code is used as an indication of the phase of the 375 µs stuffing opportunity cycle (see Table 7-1).

Table 7-1 shows that a trailer containing 13 nibbles is used in the first frame of the 375 µs stuffing opportunity cycle. A trailer of 14 nibbles is used in the second frame. The third frame provides a nibble stuffing opportunity. A trailer containing 14 nibbles is used in the third frame if a stuff occurs. If not, the trailer will contain 13 nibbles.

TABLE 7-1/G.804

Cycle/stuff counter definition

C1 code	Frame phase of cycle	Trailer length
11111111	1	13
00000000	2	14
01100110	3 (no stuff)	13
10011001	3 (stuff)	14

7.2.5.5 PLCP path status (G1)

The PLCP path status is allocated to convey the received PLCP status and performance to the transmitting far-end. This octet permits the status of the full receive/transmit PLCP path to be monitored at either end of the path. Figure 7-2 illustrates the G1 octet subfields: a 4-bit Far-End Block Error (FEBE), a 1-bit Remote Alarm Indication (RAI), and 3 X bits (X bits are set to all ones at the transmitter and may be ignored at the receiver). The use of the PLCP path status octet G1 for the Far-End Receive Failure (FERF) is for further study.

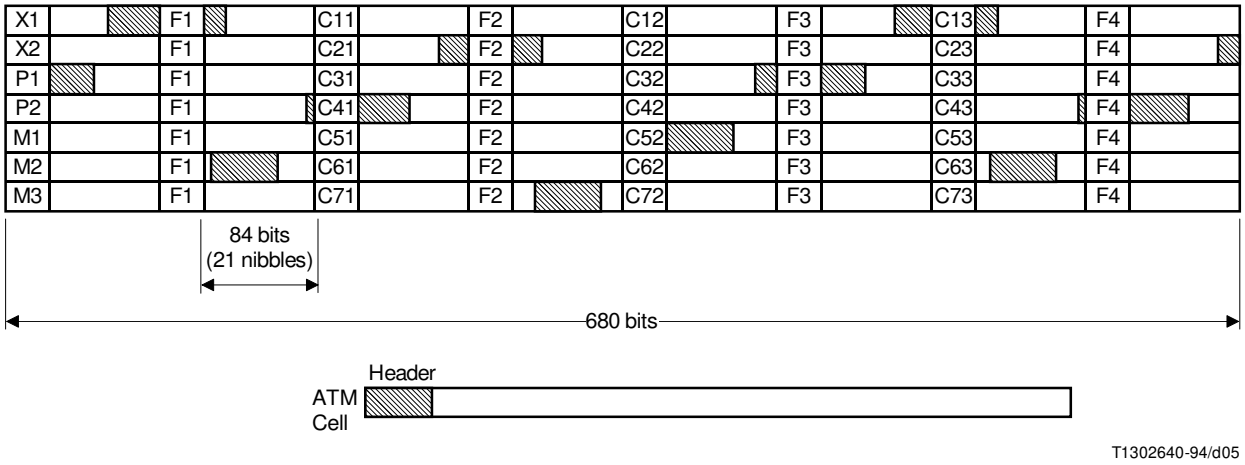


FIGURE 7-2/G.804

Frame structure for 44 736 kbit/s used to transport ATM cells

7.2.5.6 Path overhead identifier (P00-P11)

The path overhead identifier (POI) indexes the adjacent path overhead (POH) octet of the PLCP. Table 7-2 provides the coding for each of the P00-P11 octets.

7.2.5.7 Growth octets (Z1-Z6)

The growth octets are reserved for future use. These octets are set to Zi-00000000, by the transmitter (i = 1, 2, ..., 6). The receiver shall be capable of ignoring the value contained in these fields.

7.2.5.8 Trailer nibbles

The contents of each of the 13/14 trailer nibbles shall be 1100.

7.3 HEC-based mapping of ATM into 44 736 kbit/s

7.3.1 Mapping of ATM cells into 44 736 kbit/s multiframe

The ATM cells are mapped into the payload with the octet structure of the cells aligned with the nibble structure of the multiframe. The multiframe is organized such that 84 bits of payload follow every overhead bit. The 84 bits can be assumed to be organized into 21 consecutive nibbles. The ATM cell is placed such that the start of a cell always coincides with the start of a nibble. ATM cells may cross multiframe boundaries (see Figure 7-2).

7.3.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in 4.4/I.432, when no valid cells are available from the ATM layer.

7.3.3 Header error control (HEC) generation

The header error control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.

7.3.4 Cell delineation

The cell delineation shall be performed using the header error control (HEC) mechanism defined in Recommendation I.432.

7.3.5 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.

All the physical layer cells shall be discarded and only valid cells are passed to the ATM layer.

7.3.6 Physical layer OAM

The error detection and performance reporting functions of the multiframe format described in Annex A are used.

TABLE 7-2/G.804

Cycle/stuff counter definition

POI	POI code	Associated POH
P11	00101100	Z6
P10	00101001	Z5
P09	00100101	Z4
P08	00100000	Z3
P07	00011100	Z2
P06	00011001	Z1
P05	00010101	X
P04	00010000	B1
P03	00001101	G1
P02	00001000	X
P01	00000100	X
P00	00000001	C1
X Receiver ignores		

8 Mapping of ATM cells into 97 728 kbit/s

8.1 Frame format

The basic frame structure at 97 728 kbit/s, as described in Recommendation G.832, shall be used.

The ATM cells are mapped into the 756 octets of the C3 inside the 97 728 kbit/s frame with the octet structure of the cell aligned with the octet structure of the payload.

8.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the 97 728 kbit/s frames is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

8.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.

8.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the C3. In the reverse operation, following termination of 97 728 kbit/s signal, the ATM cell payload will be descrambled before being passed to ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 97 728 kbit/s frame alignment word.

8.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.

8.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

8.7 Physical layer OAM

The OAM functionality is performed using the overhead bytes defined in Recommendation G.832.

9 Mapping of ATM cells into 139 264 kbit/s

9.1 Frame format

The basic frame structure at 139 264 kbit/s, as described in Recommendation G.832, shall be used.

The ATM cells are mapped into the 2160 payload octets of the 139 264 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 9-1).

9.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432, when valid cells are not available from the ATM layer.

9.3 Header Error Control (HEC) generation

The HEC value is generated and inserted in the specific field in compliance with Recommendation I.432.

9.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into 139 264 kbit/s signal. In the reverse operation, following termination of 139 264 kbit/s signal, the ATM cell payload will be descrambled before being passed to ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 139 264 kbit/s frame alignment word.

9.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.

9.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

9.7 Physical layer OAM

The OAM functionality is performed using the overhead bytes defined in Recommendation G.832.

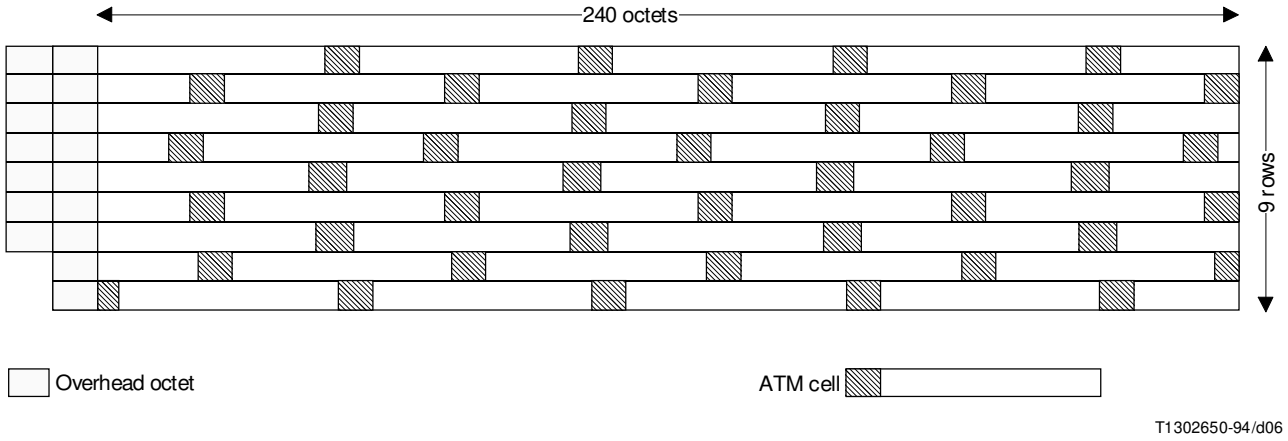


FIGURE 9-1/G.804

Frame structure at 139 264 kbit/s

Annex A

Multiframe structure of 44 736 kbit/s signal

(This annex forms an integral part of this Recommendation)

A.1 Basic frame structure at 44 736 kbit/s

A.1.1 Multiframe length

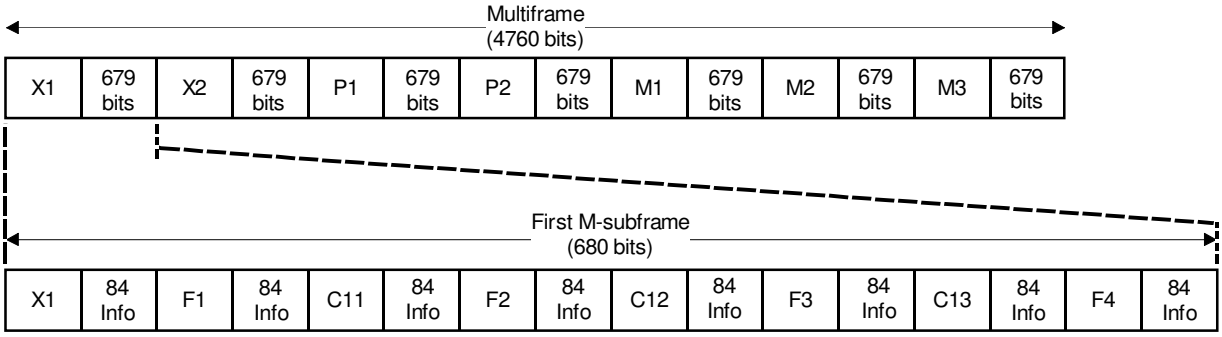
The number of bits per multiframe is 4760 bits.

A.1.2 Multiframe overhead bits

The multiframe are divided into seven M-subframe each with 680 bits; each M-subframe is further divided into eight blocks of 85 bits: one bit for overhead and 84 bits for payload (see Figure A.1). Thus, there are 56 overhead bits per multiframe.

A.1.3 Allocation of the multiframe overhead bits

The overhead bits are the first bit of the eight 85-bit blocks in each of the seven M-subframes in a multiframe, as shown in Figure A.1. The 56 overhead bits are: two X-bits, two P-bits, three M-bits, 28 F-bits and 21 C-bits.



The 56 overhead bits sequential positions							
X1	F1	C11	F2	C12	F3	C13	F4
X2	F1	C21	F2	C22	F3	C23	F4
P1	F1	C31	F2	C32	F3	C33	F4
P2	F1	C41	F2	C42	F3	C43	F4
M1	F1	C51	F2	C52	F3	C53	F4
M2	F1	C61	F2	C62	F3	C63	F4
M3	F1	C71	F2	C72	F3	C73	F4

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FIGURE A.1/G.804

44 736 kbit/s multiframe structure

A.1.3.1 X-bits (X1, X2)

X1 and X2 are used to indicate received errored multiframes to the remote-end (remote alarm indication (RAI) signal); these bits are set to binary 1 (i.e. X1 = X2 = 1) during error free condition, and to binary 0 (i.e. X1 = X2 = 0) if loss of signal (LOS), out of frame (OOF), alarm indication signal (AIS), or slips are detected in the incoming signal. The maximum allowed rate of change of state for the X-bits is once a second; therefore, the X-bits should be set to binary 0 for a length of time equal to the length of the error condition, but rounded-up to the next integer.

A.1.3.2 P-bits (P1, P2)

P1 and P2 are used for performance monitoring; these bits carry parity information calculated over the 4704 payload bits in the preceding multiframe: P1 = P2 = 1 if the digital sum of all payload bits is one, and P1 = P2 = 0 if the digital sum of all payload bits is zero. The P-bits are calculated and may be modified at each section of a facility; therefore, the P-bits provide section performance information not end-to-end performance information.

A.1.3.3 Multiframe alignment signal (M1, M2, M3)

The multiframe alignment signal 010 (M1 = 0, M2 = 1, M3 = 0) is used to locate all seven M-subframes, within the multiframe.

A.1.3.4 M-subframe alignment signal (F1, F2, F3, F4)

The M-subframe alignment signal 1001 (F1 = 1, F2 = 0, F3 = 0, F4 = 1) is used to identify the overhead bit positions.

A.1.3.5 C-bits (C11, C12, C13, C21, ...Cij, ...C73)

In general 44 736 kbit/s signals could be:

a) unchannelized for bulk data transport; and

b) channelized for multiplex applications.

In either case, the Cij-bit positions are available for specific uses, and must be settable by 44 736 kbit/s sources. The way that these Cij-bits are used determine the features available in the 44 736 kbit/s signal, through the embedded operations channels;

– The 6312-44 736 kbit/s multiplexing application (M23), uses the C-bits to indicate justification (see Recommendation G.752).

– Both, the unchannelized application as well as the channelized C-bit parity multiplex application[1)], use the C-bits as described in A.1.3.5.1.

A.1.3.5.1 Allocation of C-bits for C-bit parity application

Regardless of the application (unchannelized or channelized) the C-bits for C-bit parity application are allocated as follows:

– C11: Application identification channel (AIC) – For C-bits parity application this bit shall be set to binary 1.

– C12: Network requirements (N_r) – Reserved for future network use. It shall be set to binary 1.

– C13: Far-end alarm and control (FEAC) bit is used for two purposes:

1) alarm signals to send alarm or status information from the far-end terminal back to the near-end terminal; and

2) control signals to initiate 44 736 kbit/s and 1544 kbit/s line loopbacks at the far-end terminal, from the near-end terminal.

   At international interfaces, initiation of control loopback signal is "optional" and the application of this functionality should be at the discretion of the respective Administrations. The FEAC signal consists of a repeating 16-bit codeword with a general format of 0xxx xxx0 1111 1111, rightmost bit transmitted first (where x can be a 1 or a 0).

   To report alarm/status conditions, the 16-bit codeword must be repeated at least ten times, or while the condition exists, whichever is longer. (Table A.1 shows the alarms/status codewords assigned). These codewords shall be transmitted only after a failure has been declared: for example, a 44 736 kbit/s AIS defect would be detected and then timed for several seconds before declaring AIS failure, at which time the appropriate codeword would be transmitted.

   To send loopback control commands, two codewords must be sent: the first one – repeated ten times – to activate/deactivate, the other – also repeated ten times – to specify the line number, therefore, each loopback command consists of 20-16-bit codewords. (Table A.2 shows the control codewords assigned.) Control words take precedence over alarm signals.

   When no alarm/status or control is being transmitted, the FEAC bits must be all set to binary 1.

– C21, C22, C23: Not used; must be set to binary 1.

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1) The C-bit parity multiplex application for channelized signals uses a two-step multiplexing process to multiplex primary rate signals (1544 or 2048 kbit/s) to the 44 736 kbit/s level. In the first step, four 1544 kbit/s or three 2048 kbit/s lines are multiplexed together to form an integral signal at a bit rate f_e, (pseudo-6312 kbit/s level). In the second step, seven pseudo-6312 kbit/s level – each at a bit rate f_e – are multiplexed together to form a 44 736 kbit/s signal with enhanced operations features. The bit rate f_e (nominally 6 306.2723 kbit/s) is chosen such that when the seven pseudo-6312 kbit/s level signals are combined, along with "full time" 44 736 kbit/s level justification and the 56 frame overhead bits, the resultant output bit rate will nominally be 44 736 kbit/s. This multiplexing process is the same as that defined for the M23 application except that in the C-bit parity case all seven intermediate timeslots, one in each of the seven M-subframes, are justified at every justification opportunity. Since justification occurs 100% of the time, the C-bits are not needed to denote justification and they can be used for other purposes.

– C31, C32, C33: CP-bits are used to carry path (end-to-end facility) parity information. The network terminating equipment (NTE) that originates the 44 736 kbit/s signal must set these bits (C31 = C32 = C33) to the same value as the P-bits. The CP-bits must not be modified along the 44 736 kbit/s facility path.

– C41, C42, C43: FEBE-bits are used to carry far-end block error information. All three FEBE bits are set to binary 1 (C41 = C42 = C43 = 1) if no errors are detected in the M-bits, or F-bits, or indicated by the CP-bits. If any error condition (errored M-bits, errored F-bits, or parity in CP-bits) is detected within the multiframe, the FEBE bits must be set to any combination of 1s or 0s (except 111).

– C51, C52, C53: DL_t-bits are used for a 28.2 kbit/s terminal-to-terminal path maintenance data link. The implementation of this data link is optional but if implemented, it shall conform to the rules set forth in this subsection. The messages carried in the path maintenance data link utilize the frame structure, field definitions, and elements of procedure of the LAPD protocol defined in Recommendation Q.921 but with different addresses. The structure of the LAPD message-oriented signals is defined in Table A.3. Table A.4 shows the contents and structure of the information field for each of the four message types defined: common language path ID, ITU-T path ID, test ID, and idle signal ID. The information field contains six data elements to identify:

  1) the test type;

  2) the equipment type;

  3) the central office location;

  4) the frame (within the central office);

  5) the unit (within the frame); and

  6) information specific to the test type.

  These signals shall be transmitted continuously at a minimum rate of once per second. When LAPD messages are not being transmitted (i.e. the data link is idle), LAPD flags (01111110) shall be continuously transmitted. If terminal-to-terminal data link function is not implemented, all three bits shall be set to binary 1 (C51 = C52 = C53 = 1). Other applications for the path maintenance data link are for further study.

– C61, C62, C63: Not used; must be set to binary 1.

– C71, C72, C73: Not used; must be set to binary 1.

A.1.3.6 Special patterns used at 44 736 kbit/s

Two special patterns are defined for the 44 736 kbit/s signals independently of how the C-bits are used: AIS and IDLE, as described next.

A.1.3.6.1 Alarm indication signal (AIS)

The AIS is a signal with valid multiframe and M-subframe alignment signals, and valid P-bits. The information bits are set to a 1010... sequence, starting with a binary one (1) after each M-bit, F-bit, X-bit, P-bit and C-bit. The C-bits are set to binary zero (C1 = 0, C2 = 0, C3 = 0). The X-bits are set to binary one (X1 = 1, X2 = 1).

A.1.3.6.2 Idle signal (idle)

The idle signal is a signal with valid multiframe and M-subframe alignment signals, and valid P-bits. The information bits are set to a 1100... sequence, starting with a binary one (1) after each M-bit, F-bit, X-bit and C-bit. The C-bits are set to binary zero (C1 = 0, C2 = 0, C3 = 0), in the third M-subframe (C31, C32, C33); the remaining C-bits (three C-bits in M-subframes 1, 2, 4, 5, 6 and 7) may be individually set to one or zero, and may vary with time. The X-bits are set to binary one (X1 = 1, X2 = 1).

TABLE A.1/G.804

FEAC alarm/status codewords

FEAC alarm/status codewords	
Alarm/status condition	Codeword
Out of frame at 44 736 kbit/s	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
Equipment failure at 1544 kbit/s or 2048 kbit/s (NSA)	0 0 0 0 0 1 1 0 1 1 1 1 1 1 1 1
Equipment failure at 1544 kbit/s or 2048 kbit/s (SA)	0 0 0 0 1 0 1 0 1 1 1 1 1 1 1 1
LOS/HBER at 44 736 kbit/s	0 0 0 1 1 1 0 0 1 1 1 1 1 1 1 1
Equipment failure at 44 736 kbit/s (NSA)	0 0 0 1 1 1 1 0 1 1 1 1 1 1 1 1
Multiple LOS/HBER at 1544 k/bits or 2048 k/bits	0 0 1 0 1 0 1 0 1 1 1 1 1 1 1 1
AIS received at 44 736 kbit/s	0 0 1 0 1 1 0 0 1 1 1 1 1 1 1 1
Equipment failure for 44 736 kbit/s (SA)	0 0 1 1 0 0 1 0 1 1 1 1 1 1 1 1
Idle received at 44 736 kbit/s	0 0 1 1 0 1 0 0 1 1 1 1 1 1 1 1
Common equipment (NSA)	0 0 1 1 1 0 1 0 1 1 1 1 1 1 1 1
Single LOS/HBER at 1544 kbit/s or 2048 kbit/s	0 0 1 1 1 1 0 0 1 1 1 1 1 1 1 1

NOTES

1 The rightmost bit of each code word is transmitted first.

2 SA denotes service affecting equipment failure forcing out of service state, indicating a defect requiring immediate attention.

3 NSA denotes non-service affecting equipment failure indicating a defect in equipment that is not activated, not available, or suspended; it requires attention, but not high priority.

TABLE A.2/G.804

FEAC control codewords

FEAC control codewords	
Command	Codeword
Activate loopback	0 0 0 0 1 1 1 0 1 1 1 1 1 1 1 1
Deactivate loopback	0 0 1 1 1 0 0 0 1 1 1 1 1 1 1 1
44 736 kbit/s line	0 0 1 1 0 1 1 0 1 1 1 1 1 1 1 1
All 1544 kbit/s or 2048 kbit/s lines	0 0 1 0 0 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 1	0 1 0 0 0 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 1	0 1 0 0 0 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 1	0 1 0 0 0 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 1	0 1 0 0 1 0 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 2	0 1 0 0 1 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 2	0 1 0 0 1 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 2	0 1 0 0 1 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 2	0 1 0 1 0 0 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 3	0 1 0 1 0 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 3	0 1 0 1 0 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 3	0 1 0 1 0 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 3	0 1 0 1 1 0 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 4	0 1 0 1 1 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 4	0 1 0 1 1 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 4	0 1 0 1 1 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 4	0 1 1 0 0 0 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 5	0 1 1 0 0 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 5	0 1 1 0 0 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 5	0 1 1 0 0 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 5	0 1 1 0 1 0 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 6	0 1 1 0 1 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 6	0 1 1 0 1 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 6	0 1 1 0 1 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 6	0 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 1, Group # 7	0 1 1 1 0 0 1 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 2, Group # 7	0 1 1 1 0 1 0 0 1 1 1 1 1 1 1 1
1544 kbit/s or 2048 kbit/s Line No. 3, Group # 7	0 1 1 1 0 1 1 0 1 1 1 1 1 1 1 1
1544 kbit/s Line No. 4, Group # 7	0 1 1 1 1 0 0 0 1 1 1 1 1 1 1 1

NOTES

1 The commands that refer to 1544 kbit/s or 2048 kbit/s line apply only to a channelized C-bit parity applications.

2 “Group” refers to the four 1544 kbit/s or three 2048 kbit/s signals that form the intermediate internal f_e signal [see footnote 1)]; seven of these groups (plus justification) are combined to form the 44 736 kbit/s signal.

3 The rightmost bit of each code word is transmitted first.

4 To activate or deactivate loopback, the appropriate activate or deactivate 16-bit codeword is transmitted ten times followed immediately by ten repetitions of the 16-bit codeword that corresponds to the line number for which loopback is to be activated or deactivated. Thus, the total length of loopback control message is 20- 16-bit words.

TABLE A.3/G.804

LAPD message structure

Octet No.	Octet Label			Octet Content
1	FLAG			01111110_2
2	SAPI	CR	EA	00111100_2 or 00111110_2
3	TEI		EA	00000001_2
4	CONTROL			00000011_2
	INFORMATION FIELD			I – Path Identifier (CL or ITU-T), – Idle Signal Id, or I – Test Signal Id. I – (see Table A.4)
N – 1	FCS			See below
N	FCS			

FLAG	INTERPRETATION
01111110_2	Response Message
SAPI/CR/EA	**INTERPRETATION**
00111100_2	SAPI = 15, C/R = 0 (DTE), EA = 0
00111110_2	SAPI = 15, C/R = 1 (carrier), EA = 0
TEI/EA	**INTERPRETATION**
00000001_2	TEI = 0, EA = 1
CONTROL	**INTERPRETATION**
00000011_2	Fixed value: Unacknowledged Information Transfer
INFORMATION FIELD	**INTERPRETATION**
variable	See Table A.4
FCS	**INTERPRETATION**
Frame Check Sequence	CRC-16 Frame Check Sequence, 16-bit code

NOTE – The source of the identification messages shall generate the FCS and the zero stuffing required for transparency. Zero stuffing by a transmitter prevents the occurrence of the flag pattern (01111110) in the bits between the opening and closing flags of a frame, by inserting a zero after any sequence of five consecutive ones. The receiver removes a zero following five consecutive ones.

TABLE A.4/G.804

Information field contents for data link messages

CL Path Identification

Data elements	Binary value	
Type	0011 1000 (1 octet)	CL Path ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
CL-Facility ID	xxxx xxxx (38 octets)	CL-Facility ID

ITU-T Path Identification

Data elements	Binary value	
Type	0011 1111 (1 octet)	ITU-T Path ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
ITU-T-Facility ID	xxxx xxxx (44 octets)	ITU-T-Facility ID

IDLE Signal Identification

Data elements	Binary value	
Type	0011 0100 (1 octet)	IDLE Signal ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
Port No.	xxxx xxxx (38 octets)	Port No.

TEST Signal Identification

Data elements	Binary value	
Type	0011 0010 (1 octet)	TEST Signal ID
LIC	xxxx xxxx ... (10 octets)	Equipment ID
FIC	xxxx xxxx ... (11 octets)	Location ID
EIC	xxxx xxxx ... (10 octets)	Frame ID
Unit	xxxx xxxx ... (6 octets)	Unit ID
GEN No.	xxxx xxxx (38 octets)	Generator No.

Location	Uniquely identifies the city and building where the equipment is located.
Frame ID	Uniquely identifies the floor, aisle and bay (within the building) where the equipment is located.
Unit ID	Uniquely identifies the shelf and slot (within the frame) where the card (which generates the signal) is located.
CL-facility ID	Identifies a specific 44 736 kbit/s path, using common language conventions and codes.
ITU-T-facility ID	Identifies a specific 44 736 kbit/s path using Recommendation M.1400 conventions and codes for facility designation.
Port No.	Identifies the equipment port number that initiates the idle signal.
Generator No.	Identifies the equipment generator number that initiates the test signal.

NOTE – The null character, as defined in Recommendation T.50, shall be used to indicate the end of the string when the full length of the data field is not needed for a given element. The remaining bit positions of the data element may contain ones, zeros, or any combination of ones and zeros. In those cases where a data element is not needed for a given message, the first octet of the data element shall contain the null character, the remaining bit positions may contain ones, zeros or any combination of ones and zeros.